REVISION HISTORY

Revision	Description	Issue Date
Rev. 0.1	Initial Issue	Mar. 07. 2012
Rev. 0.2	Added THD+N vs. Output Power	Mar. 20. 2012
Rev. 0.3	Added Demo Board Application Artwork data	Mar. 26. 2012
Rev. 0.4	Added AP Test Data	Apr. 10. 2012
Rev. 1.0	Release datasheet	Apr. 11. 2012
Rev. 1.1	Promote LY8009VL Product only.	Apr. 19. 2012
Rev. 1.2	Modify ESOP8 package (del dual pad item)	Dec. 25. 2013
	修改PKG 內部參數	Oct. 06. 2014
Rev. 1.3	Modify ORDERING INFORMATION Modify PACKAGE OUTLINE DIMENSION	May. 25. 2015
Rev. 1.4	Page2 (Low enable the device) modify to (Low shutdown the device)	Apr. 24. 2023
Rev. 1.5	Added Package : 10pin 118mil MSOP(Page 1) Added PIN DESCRIPTION MSOP10 (Page2) Added ORDERING INFORMATION MSOP10 (Page3) Added MSOP10 PACKAGE OUTLINE DIMENSION(Page19)	Jan.12.2024

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FEATURES

- 5.5W Into 2Ω from 5.5V power supply at THD+N = 10% (Typ).
- 3.6W Into 4Ω from 5.5V power supply at THD+N = 10% (Typ).
- 2.5V~5.5V power supply.
- Low shutdown current.
- Low quiescent current.
- Short-circuit protection and automatic recovery.
- Over-heat protection and automatic recovery.
- Minimum external components.
- No output filter required for inductive loads.
- Low noise during turn-on and turn-off transitions.
- Lead free and green package available. (RoHS Compliant)
- Package : LY8009V 8pin 150mil ESOP.
  LY8009U 10pin 118mil MSOP

APPLICATION

- Portable electronic devices
- USB audio, Audio System.
- Mini combo system, PDAs

GENERAL DESCRIPTION

The LY8009 is a high efficiency, 5.5W mono class D audio power amplifier. It is a low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplify design.

The LY8009 is designed to meet of portable electronic devices and mini speaker system. There exist 2 sets of outputs for a single input on LU8098U to drivie 2 separated speakers. In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the LY8009..

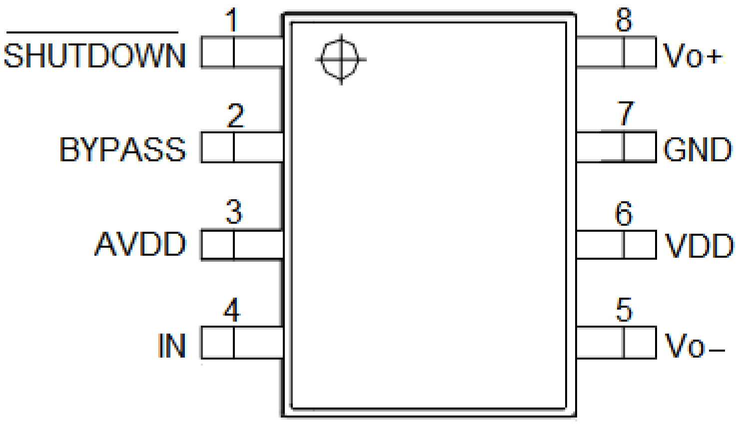
The device is a single 5.5V power supply, it is capable of driving 2Ω speaker load at a continuous average output of 5.5W with 10% THD+N.

The gain of the LY8009 is externally configurable which allows independent gain control from multiple sources by summing the signals.

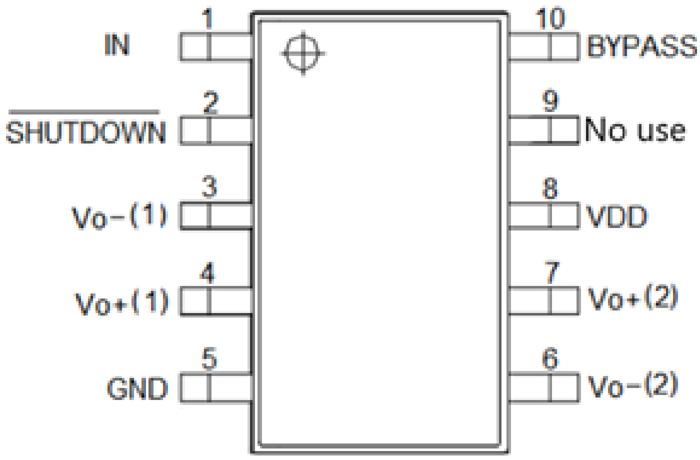
The device also features an internal thermal shutdown protection and output pin short circuit protection prevent the device from damage during fault conditions.

PIN CONFIGURATION

LY8009V ESOP8 Pin Configuration (Top View)



LY8009U MSOP10 Pin Configuration
(Top View)



PIN DESCRIPTION

SYMBOL	Pin No. ESOP	DESCRIPTION of LY8009V
SHUTDOWN	1	Shutdown control pin.(**Low** shutdown the device)
BYPASS	2	Bypass pin.
AVDD	3	Analog power supply.
IN	4	Audio input pin.
Vo-	5	Negative BTL output.
V_{DD}	6	Power supply.
GND	7	Ground.
Vo+	8	Positive BTL output.

SYMBOL	Pin No. MSOP	DESCRIPTION of LY8009U
INR	1	Input channel.
Shutdown	2	Shutdown control pin.(when **Low** level is shutdown mode)
Vo-(1)	3	Negative (-) BTL output. channel 1.
Vo+(1)	4	Positive (+) BTL output. channel 1.
GND	5	Ground.
Vo-(2)	6	Negative (-) BTL output. channel 2.
Vo+(2)	7	Positive (+) BTL output. channel 2.
V_{DD}	8	Power supply
No use	9	Empty pin
BYPASS	10	Bypass pin

ORDERING INFORMATION

Ordering Code	Packing Type	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)	Input Type	Output Type
LY8009VLT	Tape&Reel	Mono	ESOP8	5.5W/2Ω @5.5V_BTL 4.5W/3Ω @5.5V_BTL 3.6W/4Ω @5.5V_BTL 2.0W/8Ω @5.5V_BTL	SE	BTL
LY8009ULT	Tape&Reel	Mono	MSOP10	5.5W/2Ω @5.5V_BTL 4.5W/3Ω @5.5V_BTL 3.6W/4Ω @5.5V_BTL 2.0W/8Ω @5.5V_BTL	SE	BTL (2 sets)

***1 ESOP → with thermal pad.**

APPLICATION CIRCUIT

Figure 1a. LY8009V Application Circuit

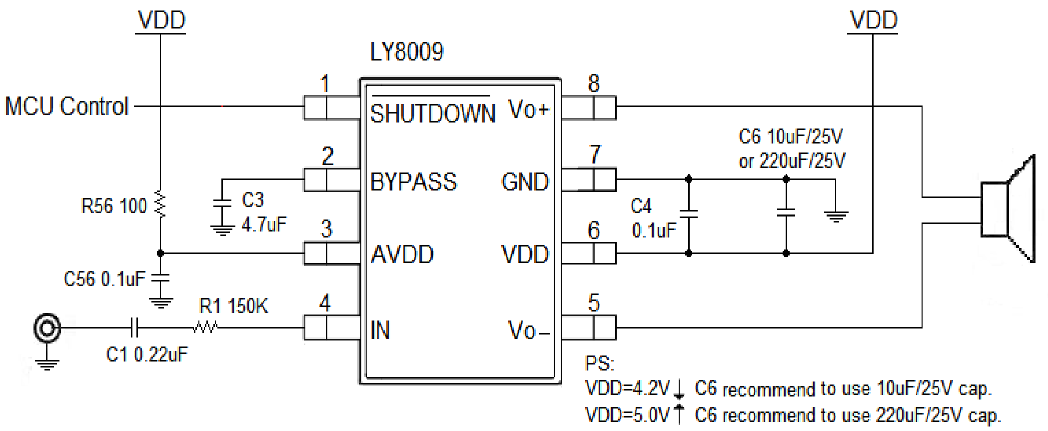


Figure 1b. LY8009U Application Circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6.0	V
Operating Temperature	T_A	-40 to 85 (I grade)	℃
Input Voltage	V_I	-0.3V to V_{DD} +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

ELECTRICAL CHARACTERISTICS (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. [*2]	MAX.	UNIT
Supply voltage	V_{DD}		2.5	-	5.5	V
Quiescent Current	I_Q	V_{DD} = 5.5V, No Load	-	4.0	-	mA
		V_{DD} = 3.7V, No Load	-	3.5	-	
		V_{DD} = 2.5V, No Load	-	3.0	-	
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$ ≦0.8V, V_{DD} = 2.5V to 5.5V	-	0.1	-	μA
Shutdown voltage input high	V_{SDIH}		1.4	-	-	V
Shutdown voltage input low	V_{SDIL}		-	-	0.3	
Output offset voltage	V_{OS}	V_I = 0 V, Av = 2 V/V, V_{DD} = 2.5 V to 5.5 V	-	-	50	mV
Thermal shutdown temperature	T_{SD}	Shutdown temp.	-	145	-	℃
		Restore temp.	-	120	-	
Total Gain [*1]	G_V	V_{DD}= 2.5V to 5.5V	[150KΩ / (5KΩ+Ri)] x4			V/V

(*1)The audio amplifier's gain is determined by :

Pre-Amplifier Gain = [150KΩ / (5KΩ + Ri)] x 2

Total Gain = {[150KΩ / (5KΩ + Ri)] x 2} x 2

where Ri is the external serial resistance at the input pin.

(*2)Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and T_A = 25℃

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▪ OPERATING CHARACTERISTICS (1)(T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *2	MAX.	UNIT
Output Power	Po	THD+N= 10%, f = 1 kHz, RL= 2Ω	VDD=5.5V	-	5.5	-	W
			VDD=5.0V	-	4.5	-	
			VDD=3.7V	-	2.5	-	
			VDD=2.5V	-	1.0	-	
		THD+N= 1%, f = 1 kHz, RL= 2Ω	VDD=5.5V	-	4.5	-	
			VDD=5.0V	-	3.6	-	
			VDD=3.7V	-	2.0	-	
			VDD=2.5V	-	0.8	-	
		THD+N= 10%, f = 1 kHz, RL= 4Ω	VDD=5.5V	-	3.6	-	
			VDD=5.0V	-	3.0	-	
			VDD=3.7V	-	1.6	-	
			VDD=2.5V	-	0.7	-	
		THD+N= 1%, f = 1 kHz, RL= 4Ω	VDD=5.5V	-	2.9	-	
			VDD=5.0V	-	2.4	-	
			VDD=3.7V	-	1.3	-	
			VDD=2.5V	-	0.5	-	
		THD+N= 10%, f = 1 kHz, RL= 8Ω	VDD=5.5V	-	2.1	-	
			VDD=5.0V	-	1.7	-	
			VDD=3.7V	-	0.9	-	
			VDD=2.5V	-	0.4	-	
		THD+N= 1%, f = 1 kHz, RL= 8Ω	VDD=5.5V	-	1.6	-	
			VDD=5.0V	-	1.4	-	
			VDD=3.7V	-	0.7	-	
			VDD=2.5V	-	0.3	-	
Power supply rejection ratio	PSRR	VDD=5.0V, Input=GND. Ri=51K, Ci=0.1μF. RL=4Ohm,	f=1KHz	-	-55	-	dB
			f=217Hz	-	-54	-	
Signal-to-noise ratio	SNR	RL = 8Ω, Input=GND, 1.0W=0dB	VDD=5.0V	-	80	-	dB
Output voltage noise	Vn	VDD=5.0V,Input=GND, Load=4Ω, Ri=150K,Ci=0.1uF, f = 20 Hz to 20 kHz,		-	181	-	uV
		VDD=5.0V,Input=GND, Load=4Ω, Ri=51K,Ci=0.1uF, f = 20 Hz to 20 kHz,		-	274	-	
Efficiency	η	VDD=5.0V,f=1kHz,RL=4Ω, Output power =3.0W		-	85	-	%
		VDD=3.7V,f=1kHz,RL=4Ω, Output power =1.6W		-	85	-	
		VDD=5.0V,f=1kHz,RL=2Ω, Output power =4.5W		-	77	-	
		VDD=3.7V,f=1kHz,RL=2Ω, Output power =2.4W		-	77	-	
Frequency	Fc	VDD=2.5V~5.5V		-	210	-	kHz

■ OPERATING CHARACTERISTICS (2) (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *2	MAX.	UNIT
		Voltage	C_{bypass} Cap.				
Start-up time from shutdown	Z_I	V_{DD} = 5.0V	C_{bypass} = 4.7μF	-	200	-	ms
			C_{bypass} = 2.2μF	-	96	-	
			C_{bypass} = 1.0μF	-	84	-	
			C_{bypass} =0.47μF	-	40	-	
			C_{bypass} = 0.22μF	-	20	-	
			C_{bypass} =None	-	20	-	
		V_{DD} = 3.7V	C_{bypass} = 4.7μF	-	156	-	
			C_{bypass} = 2.2μF	-	80	-	
			C_{bypass} = 1.0μF	-	72	-	
			C_{bypass} =0.47μF	-	36	-	
			C_{bypass} = 0.22μF	-	22	-	
			C_{bypass} =None	-	20	-	

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TYPICAL PERFORMANCE CHARACTERISTICS

Note* On LY8009U the two sets of outputs are is paralleled together when measurement (VOP1// VOP2; VON1//VON2)

Figure 2

Total Harmonic Distortion + Noise vs Output Power (2Ω)

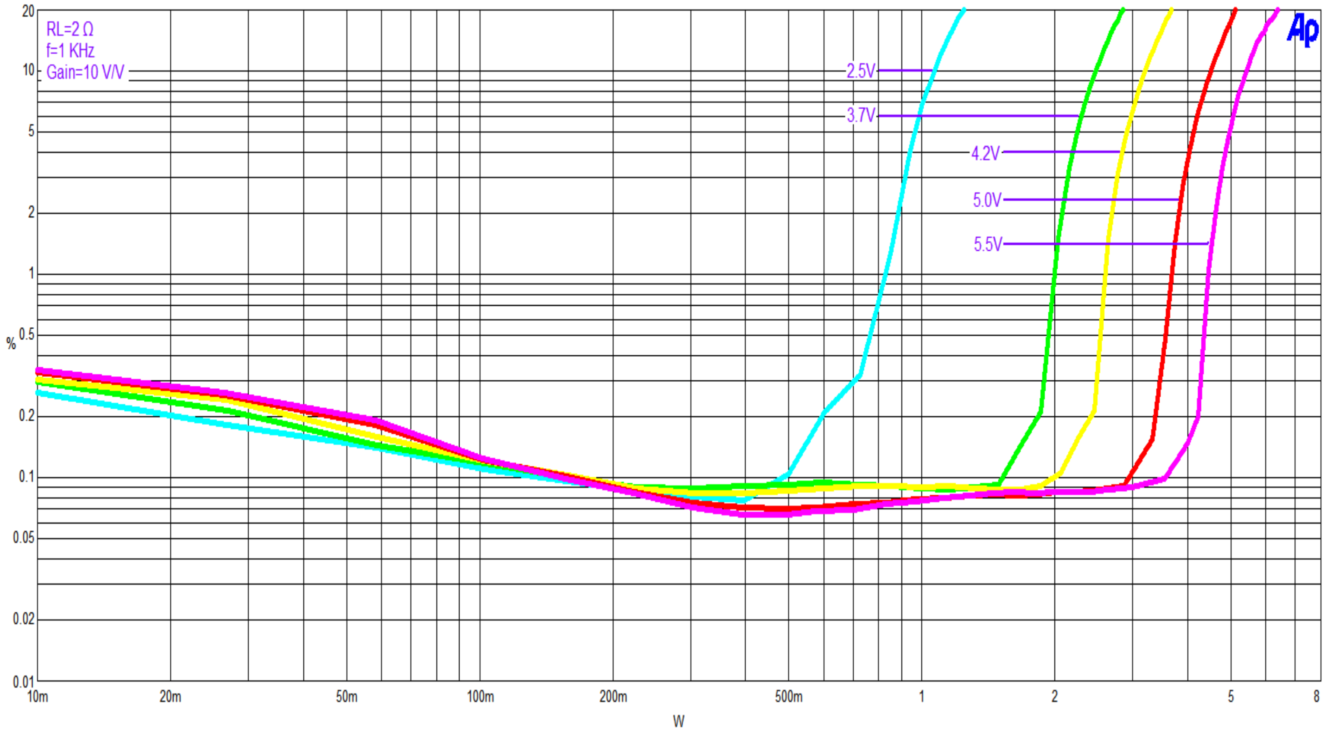

Figure 3

Total Harmonic Distortion + Noise vs Output Power (4Ω)

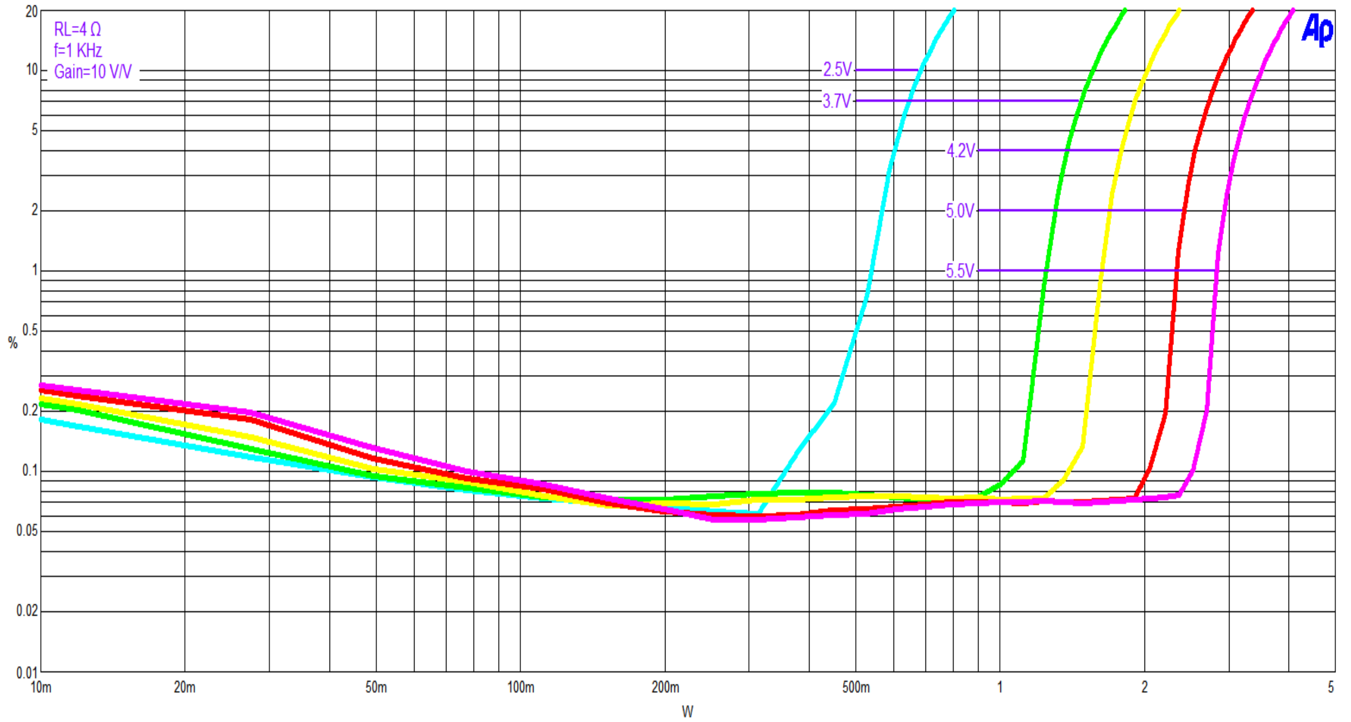

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Figure 4
Total Harmonic Distortion + Noise vs Output Power (8Ω)

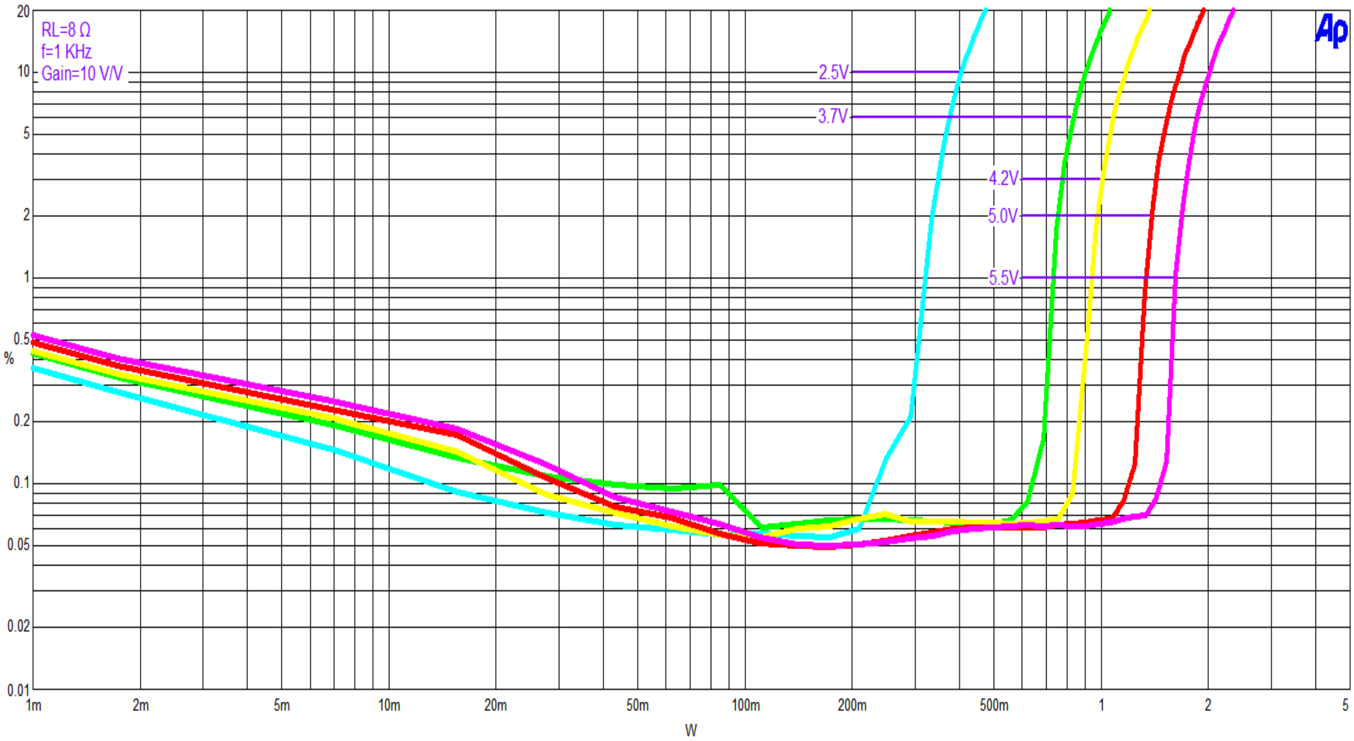
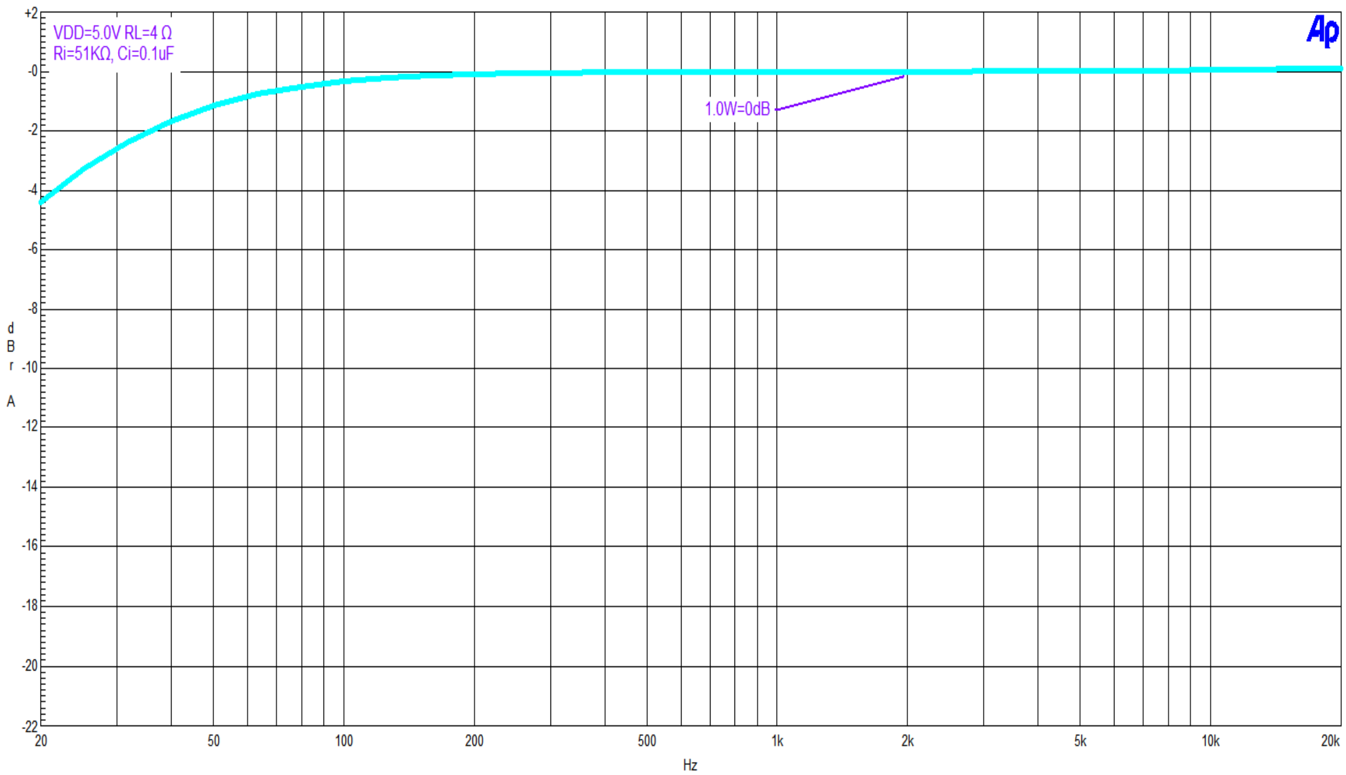
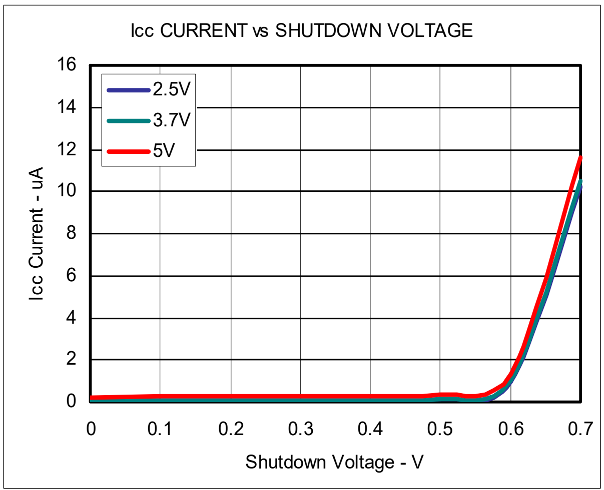


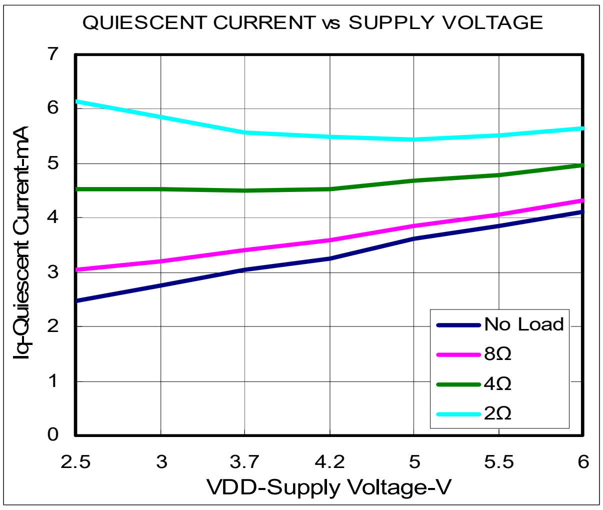
Figure 5
Frequency Response



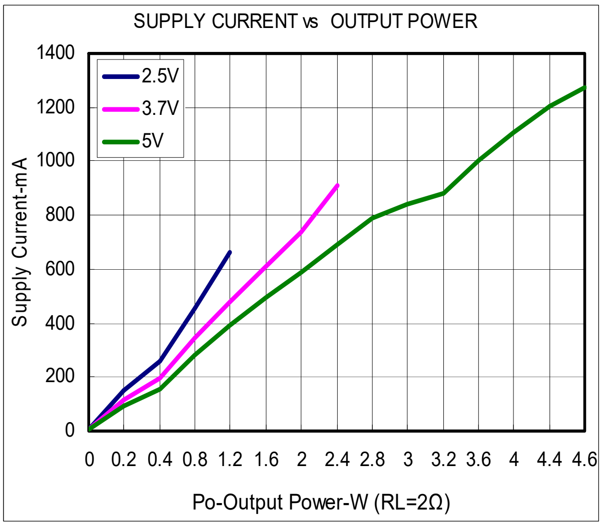
Icc Current vs. Shutdown Voltage



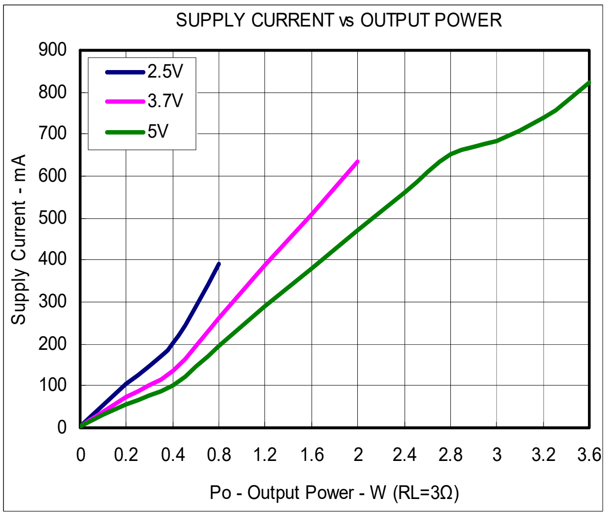
Quiescent Current vs. Supply Voltage



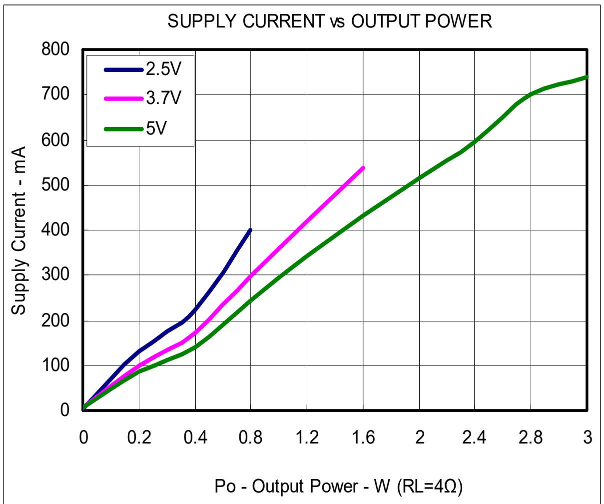
Supply Current vs. Output Power (RL=2Ω)



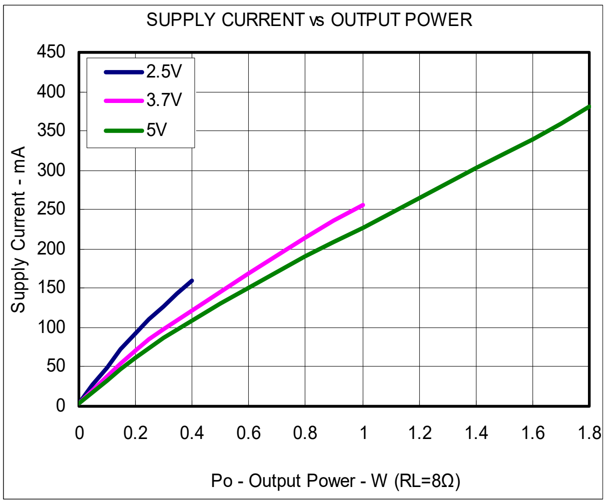
Supply Current vs. Output Power (RL=3Ω)



Supply Current vs. Output Power (RL=4Ω)



Supply Current vs. Output Power (RL=8Ω)



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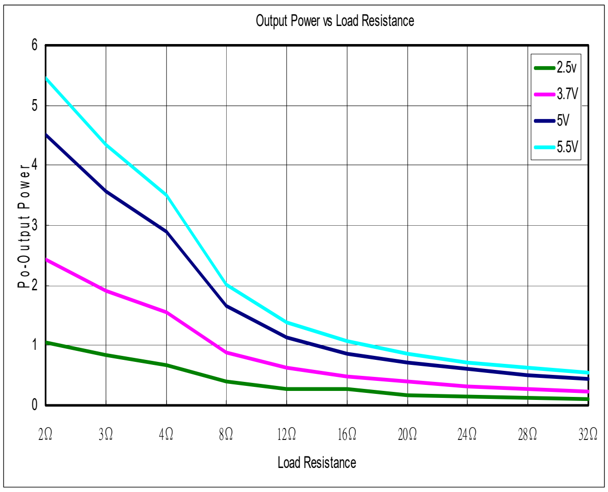
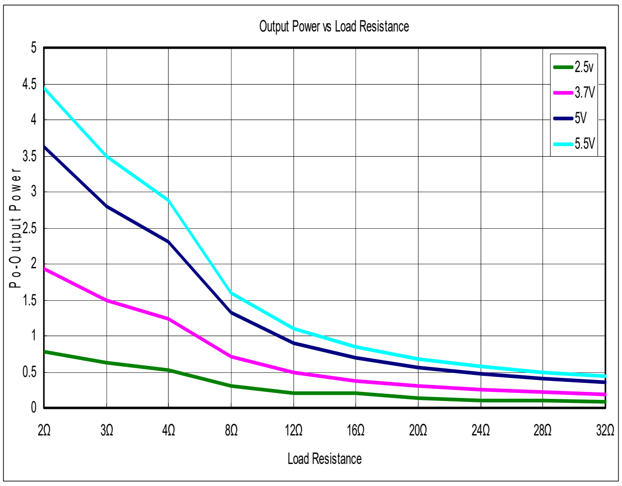
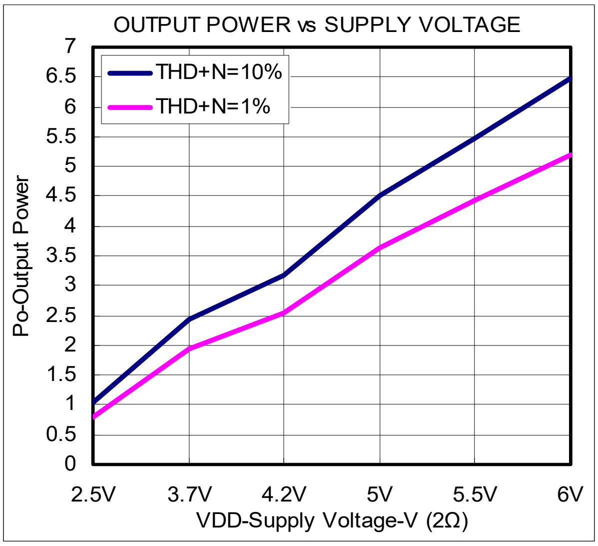
Load Resistance vs. Output Power (THD+N=10%)



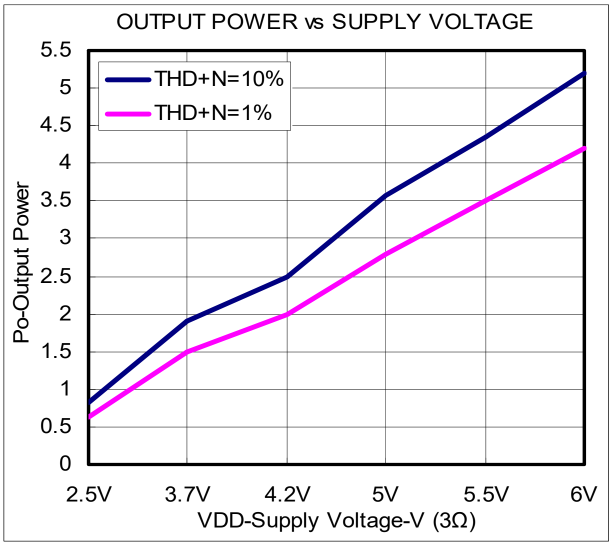
Load Resistance vs. Output Power (THD+N=1%)



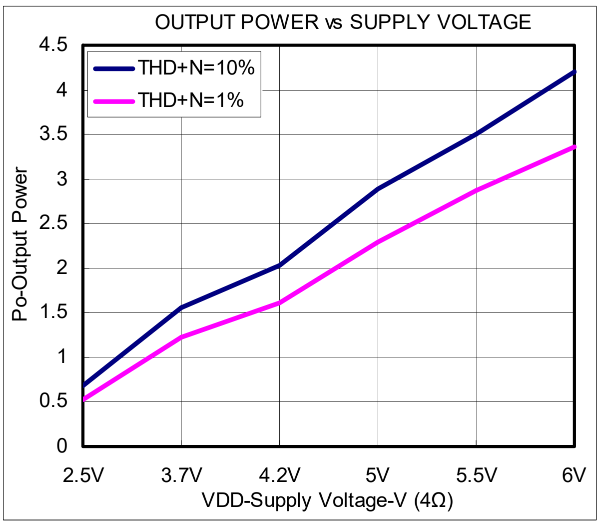
Output Power vs. VDD (RL=2Ω)



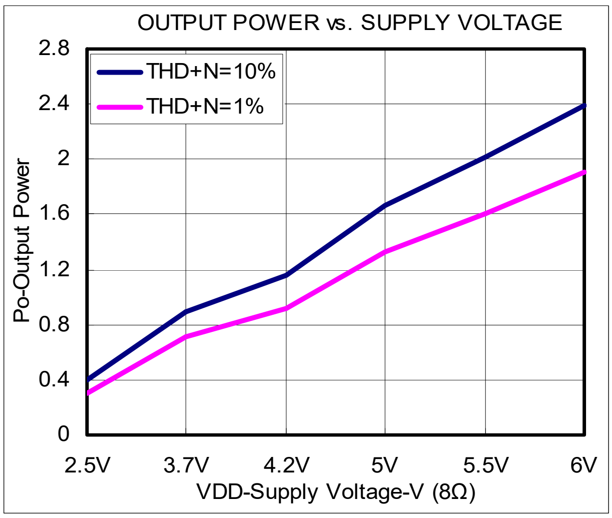
Output Power vs. VDD (RL=3Ω)



Output Power vs. VDD (RL=4Ω)



Output Power vs. VDD (RL=8Ω)



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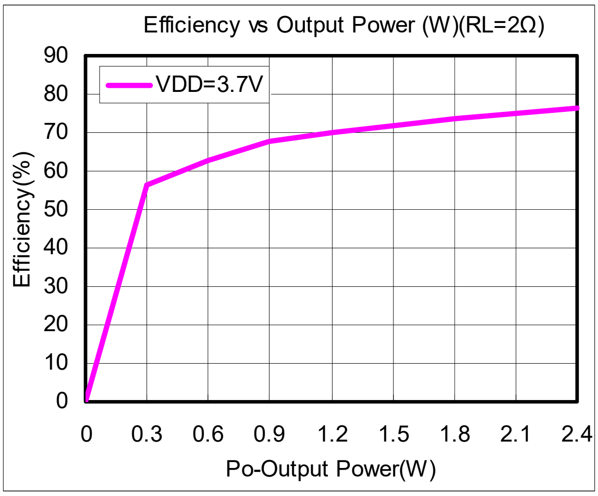
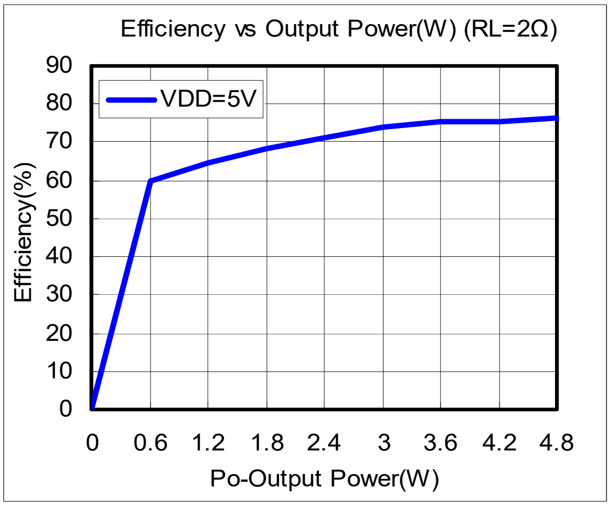
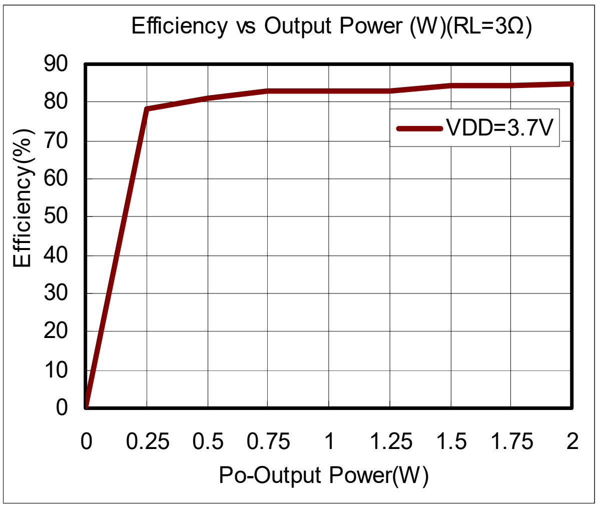
Efficiency vs. Output Power (2Ω) 3.7V



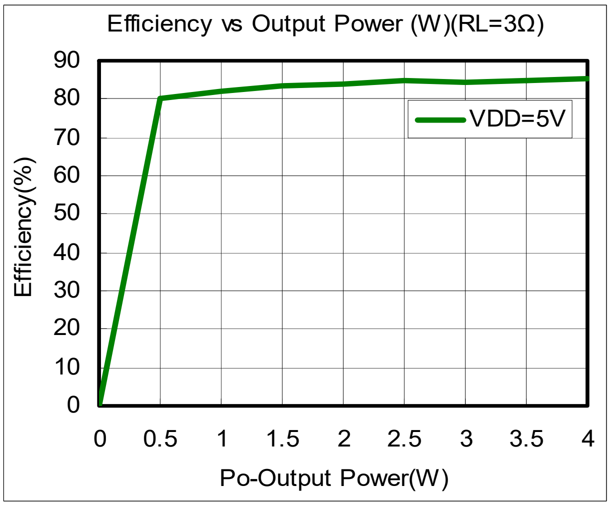
Efficiency vs. Output Power (2Ω) 5.0V



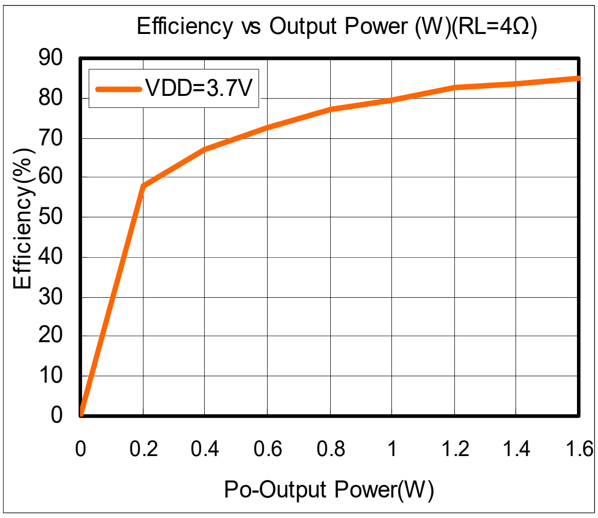
Efficiency vs. Output Power (3Ω) 3.7V



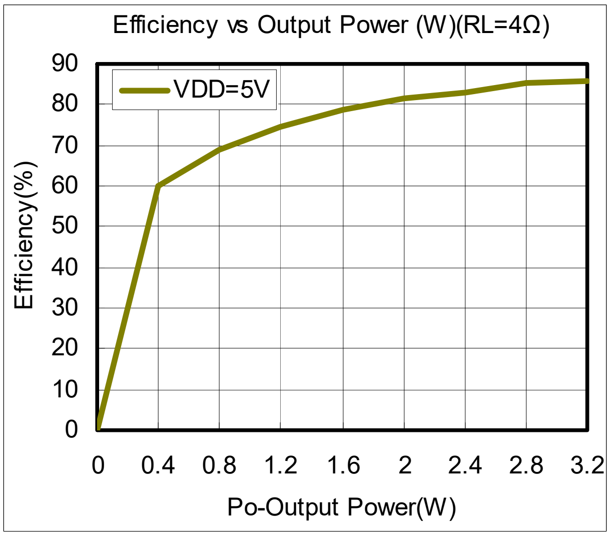
Efficiency vs. Output Power (3Ω) 5.0V



Efficiency vs. Output Power (4Ω) 3.7V



Efficiency vs. Output Power (4Ω) 5.0V



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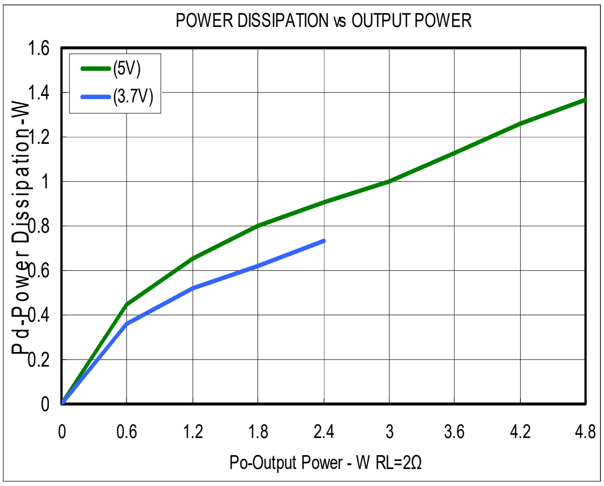
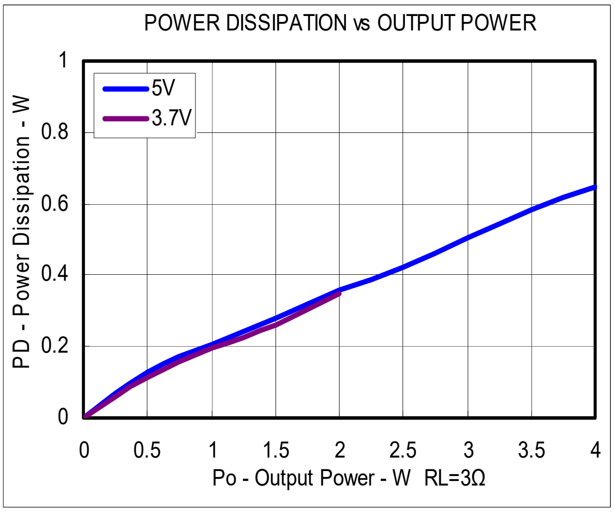
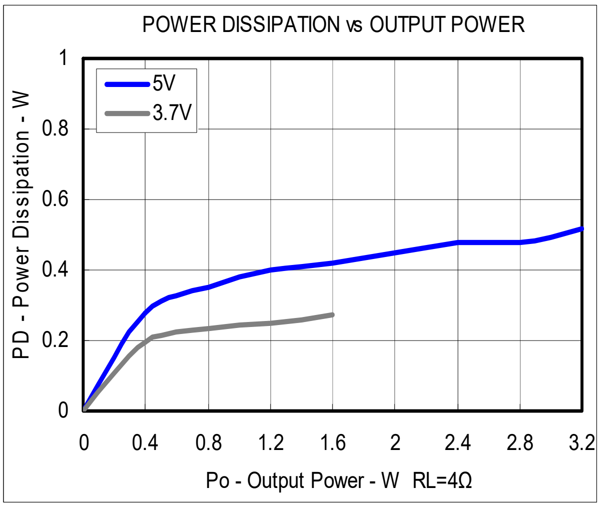
Dissipation vs. Output Power (2Ω)



Dissipation vs. Output Power (3Ω)



Dissipation vs Output Power (4Ω)



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APPLICATION INFORMATION of LY8009V

Input Resistors (Ri) and Gain

The input resistors (Ri) set the gain of the amplifier according to the equation.

Pre-Amplifier Gain = (Rf / Ri) x 2 = [150KΩ / (5KΩ + Ri)] x 2

Total Gain = [(Rf / Ri) x 2] x 2 = {[150KΩ / (5KΩ + Ri)] x 2} x 2

A_{VD} = 20 x log {2 x [(Rf /Ri) x2]}

The resistor matching is very important in the amplifiers. Balance of the output on the reference voltage depends on matched ratio of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance.
Resistor arrays with 1% matching can be used with a tolerance greater than 1%.Place the input resistors very close to the LY8009 to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the LY8009 to operate at its best,

For example

Table 1. Typical Total Gain and A_{VD} Values

Rf (KΩ)	150	150	150	150	150	150
Ri (KΩ)	300	150	100	75	50	37.5
Pre AMP. Gain	1	2	3	4	6	8
Total Gain	2	4	6	8	12	16
A_{VD} (dB)	6.02	12.04	15.56	18.06	21.58	24.08

Input Capacitors (Ci)

The LY8009 using a single-ended source, So the input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency(f_C), determined in the equation.

$f_c = 1 / (2\pi \, Ri \, Ci)$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Equation is reconfigured to solve for the input coupling capacitance.

$Ci = 1 / (2\pi \, Ri \, f_c)$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For example

In the table 2 shows the external components. Rin in connect with Cin to create a high-pass filter.

Table 2. Reference Component Values

Reference	Description	Note
Ri	150KΩ	1% tolerance resistors
Ci	0.22uF	80%/–20%

$Ci = 1 / (2\pi\, Ri\, fc)$

$Ci = 1 / (2\pi * 150K\Omega * 4.8Hz) = 0.221uF$，Use 0.22uF

Two Single-Ended Input Signals

Two resistors and two capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently.

Pre-Amplifier Gain 1 = [150KΩ / (5KΩ + Ri1)] x 2

Pre-Amplifier Gain 2 = [150KΩ / (5KΩ + Ri2)] x 2

$Ci1 = 1 / (2\pi\, Ri1\, fc1)$

$Ci2 = 1 / (2\pi\, Ri2\, fc2)$

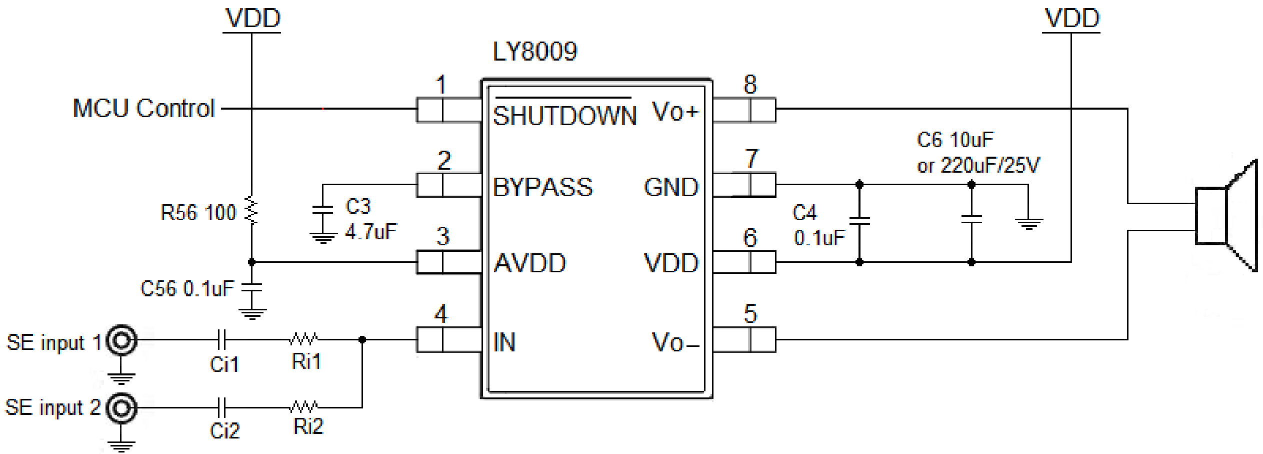

Figure 6. Application Schematic With Two Single-Ended Inputs Configuration

Bypass Capacitor (Cbypass)

The Bypass Capacitor (C3) is the most critical capacitor. During start-up or recovery from shutdown mode, Cbypass determines the rate at which the amplifier starts up. The Cbypass will to reduce noise caused by the power supply coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded the PSRR and THD+N values. The bypass capacitor (C3) with values of 1.0μF to 4.7μF is recommended for the best THD and noise performance. Therefore, increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

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Shutdown Function

When the LY8009 not in use. The device will be to turn off the amplifier to reduce power consumption. When logic low is applied to the shutdown pin, this shutdown feature will turns the amplifier off. By switching the shutdown pin connected to GND, the device supply current draw will be minimized in idle mode.

Over-Heat Protection

The LY8009 has a built-in over-heat protection circuit, it will turn off all power output when the chip temperature over 145℃, the chip will return to normal operation automatically after the temperature cool down to 120℃.

Short-circuit Protection

The LY8009 has short circuit protection circuitry on the outputs to prevent damage when output-to-output short occurs. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

PCB Layout

All the external components must place very close to the LY8009. The input resistors need to be very close to the LY8009 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the LY8009. Then place the decoupling capacitor C4, close to the LY8009 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Making the high current traces going to VDD, GND, V_{O+} and V_{O-} pins of the LY8009 should be as wide as possible to minimize trace resistance. If these traces are too thin, the LY8009's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

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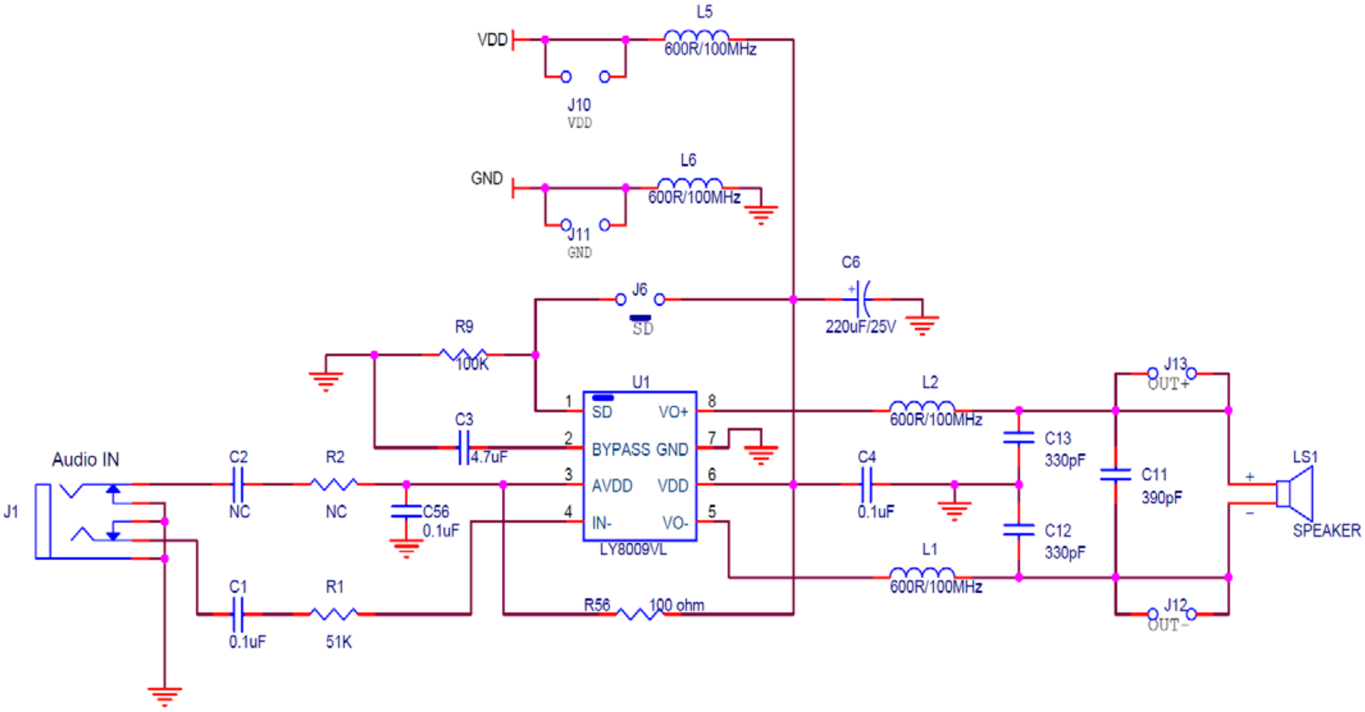
▪ DEMO BOARD INFORMATION

Demo Board Application Circuit :



Demo Board BOM List

LY8009 V1.0 BOM List

No.	Description	Reference	Note
1	Resistor, 100KΩ	R9	1/16W,1%
2	Resistor, 51KΩ	R1	1/16W,1%
3	Resistor, 100Ω	R56	1/16W,1%
4	Capacitor, 0.1uF	C1,C4,C56	80%/−20%, nonpolarized
5	Capacitor, 4.7uF	C3	80%/−20%, nonpolarized
6	Capacitor, 220.0uF	C6	25V,105℃,8x11,EC Cap.
7	IC	U1	LY8009VL, ESOP8
8	1*2 Pin Header	J6	Pitch 2.54 mm
9	Capacitor, 330pF(Option)	C12,C13	80%/−20%, nonpolarized
10	Capacitor, 390pF(Option)	C11	80%/−20%, nonpolarized
11	Chip Bead 1KΩ/100MHz(Option)	L1,L2	1000Ω(1KΩ)±25%/100MHz

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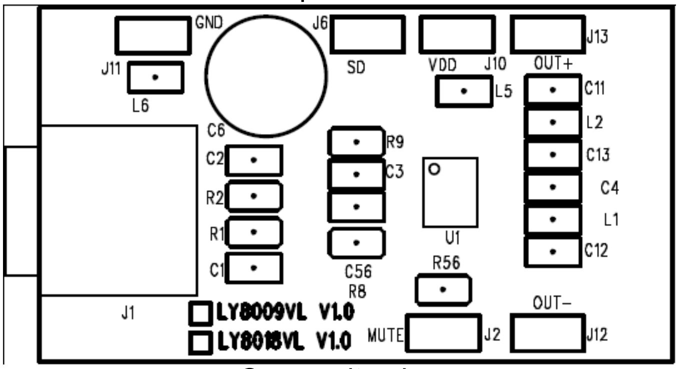
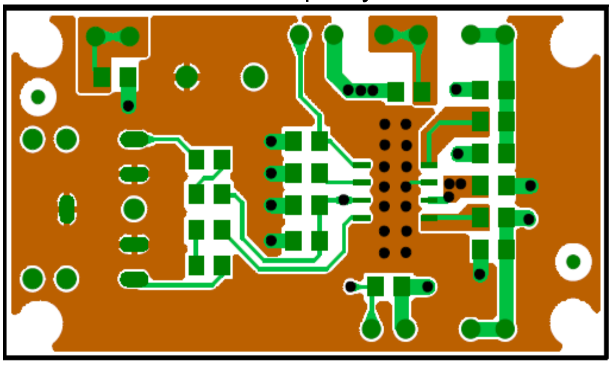
12	NC	R2,C2	No Components

LY8009V Demo Board Artwork

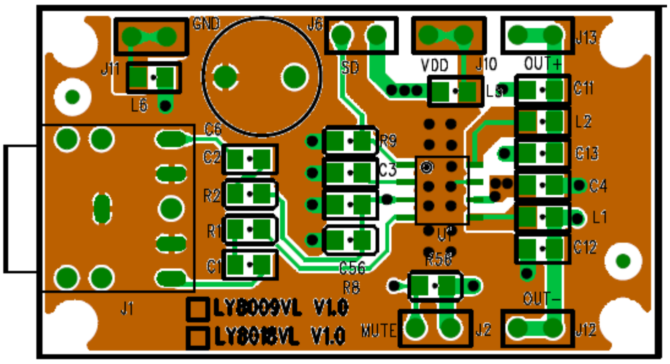
Top Silkscreen



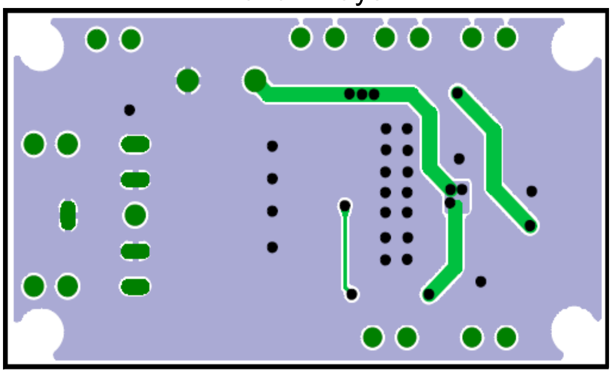
Top Layer



Composite view



Bottom Layer



▪ APPLICATION INFORMATION of LY8009U

Input Resistors (Ri) and Gain

The LY8209 have two internal amplifier stages. The pre-amplifier gain is externally configurable, while the total gain is internally fixed. The closed-loop gain of the pre-amplifier gain is set by selecting the Rf (Rf=150KΩ) to Ri while the total gain is fixed at 4x. So the input resistors (R_i) set the gain of the amplifier according to the equation.

Pre-Amplifier Gain = (Rf / Ri) x 2

Total Gain = [(Rf / Ri) x 2] x 2

A_{VD} = 20 x log [4 x (Rf /Ri)]

The resistor matching is very important in the amplifiers. Balance of the output on the reference voltage depends on matched ratio of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance.
Resistor arrays with 1% matching can be used with a tolerance greater than 1%.Place the input resistors very close to the LY8209 to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to 4 V/V or lower. Lower gain allows the LY8209 to operate at its best,

For example

Table 1. Typical Total Gain and A_{VD} Values

Rf (KΩ)	150	150	150	150	150
Ri (KΩ)	150	75	50	25	15
Pre AMP. Gain	2	4	6	12	20
Total Gain	4	8	12	24	40
A_{VD} (db)	12.04	18.06	21.58	27.60	32.04

Input Capacitors (Ci)

The LY8209 using fully differential source, So the input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency(f_c), determined in the equation.

$f_c = 1 / (2\pi R_i C_i)$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Equation is reconfigured to solve for the input coupling capacitance.

$C_i = 1 / (2\pi R_i f_c)$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For example

In the table 2 shows the external components. Rin in connect with Cin to create a high-pass filter.

Table 2. Reference Component Values

Reference	Description				Note
Ri	150KΩ		51 KΩ		1% tolerance resistors
Ci	0.22uF	0.1uF	0.22uF	0.1uF	80%/–20% non polarized
corner frequency	4.8Hz	10.6Hz	14.18Hz	31.2Hz	

$Ci = 1 / (2\pi Ri\ fc)$

$Ci = 1 / (2\pi \times 150K\Omega \times 4.8Hz)=0.221uF$，One would likely choose a value of 0.22uF as this value is commonly used.

Bypass Capacitor (Cbypass)

The Bypass Capacitor (C3) is the most critical capacitor. During start-up or recovery from shutdown mode, Cbypass determines the rate at which the amplifier starts up. The Cbypass will to reduce noise caused by the power supply coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded the PSRR and THD+N values. The bypass capacitor (C3) with values of 1.0μF to 10.0μF is recommended for the best THD and noise performance. Therefore, increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Table 3. CBYPASS Reference Component Values

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Start-up time from shutdown	Z_I	V_{DD}=5.0V, Ci=0.1uF, Ri=51KΩ, Av=11	C_{bypass} = 10.0μf	-	560	-	ms
			C_{bypass} = 4.7μf	-	300	-	
			C_{bypass} = 2.2μf	-	150	-	
			C_{bypass} = 1.0μf	-	120	-	
		V_{DD}=3.7V, Ci=0.1uF, Ri=51KΩ, Av=11	C_{bypass} = 10.0μf	-	460	-	
			C_{bypass} = 4.7μf	-	250	-	
			C_{bypass} = 2.2μf	-	135	-	
			C_{bypass} = 1.0μf	-	100	-	

Shutdown Function

When the LY8209 not in use. The device will be to turn off the amplifier to reduce power consumption. When logic low is applied to the shutdown pin, this shutdown feature will turns the amplifier off. By switching the shutdown pin connected to GND, the device supply current draw will be minimized in idle mode. The pin cannot be left floating due to the internal did not pull-up.

Over-Heat Protection

The LY8209 has a built-in over-heat protection circuit, it will turn off all power output when the chip temperature over 150℃, the chip will return to normal operation automatically after the temperature cool down to 110℃.

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Short-circuit Protection

The LY8209 has short circuit protection circuitry on the outputs to prevent damage when output-to-output short occurs. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

▪PCB LAYOUT

All the external components must place very close to the LY8209. The input resistors need to be very close to the LY8209 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the LY8209. Then place the decoupling capacitor Cs, close to the LY8209 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.
If device had AVDD(Analog VDD) pin, place the decoupling capacitor 0.1uF, close to the device pin is very important.

Making the high current traces going to VDD, GND, V_{O+} and V_{O-} pins of the LY8209 should be as wide as possible to minimize trace resistance. If these traces are too thin, the LY8209's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

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▪ DEMO BOARD INFORMATION

Demo Board Application Circuit : (Stereo Mode)

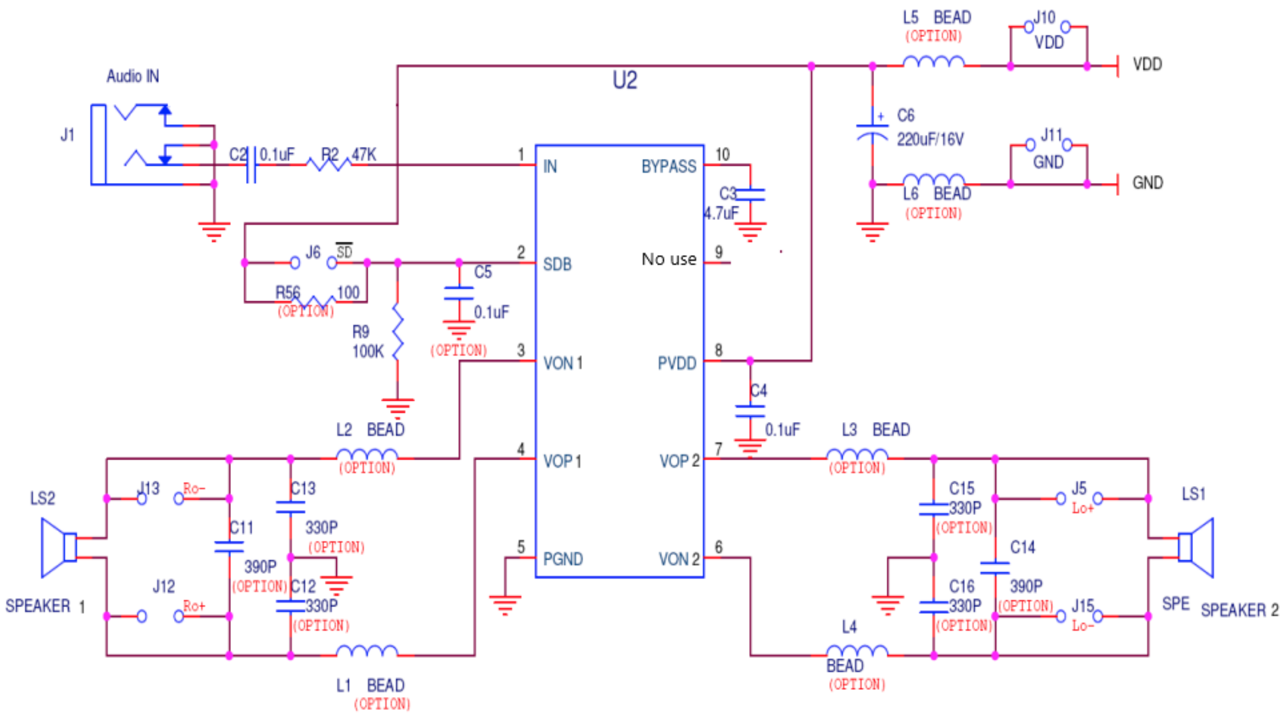

Figure 10. Demo Board Application Circuit

Demo Board BOM List :

LY8209 V1.0 BOM List (Stereo Mode)

No.	Description	Reference	Note
1	Resistor, 47KΩ	R2	1/16W,1%
2	Resistor, 100KΩ	R9	1/16W,1%
3	Capacitor, 0.1uF	C2,C4	80%/−20%, non polarized
4	Capacitor, 4.7uF	C3	80%/−20%, non polarized
5	Capacitor, 220.0uF	C6	25V,105℃,8x11,EC Cap.
6	IC	U2	LY8209U, (MSOP10)
7	1*2 Pin Header	J2,J6	Pitch 2.54 mm
8	Capacitor, 330pF(Option)	C12,C13,C15,C16	80%/−20%, nonpolarized
9	Capacitor, 390pF(Option)	C11,C14	80%/−20%, nonpolarized
10	Chip Bead 1KΩ/100MHz(Option)	L1,L2,L3,L4,L5,L6	1000Ω(1KΩ)±25%/100MHz
11	NC	R1, C1	No use

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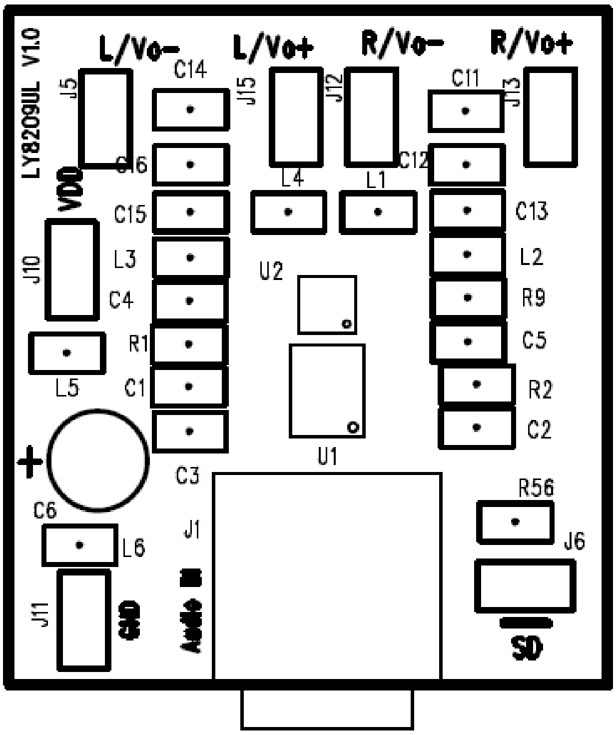
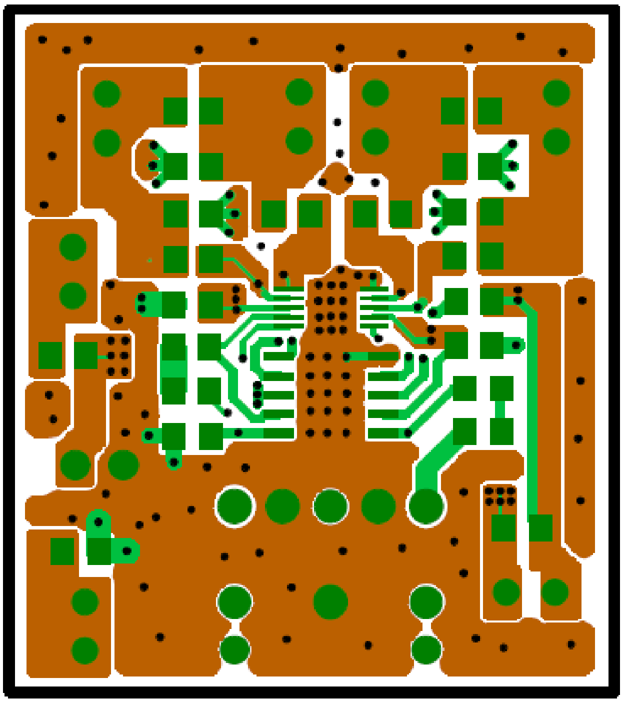
Demo Board Artwork :

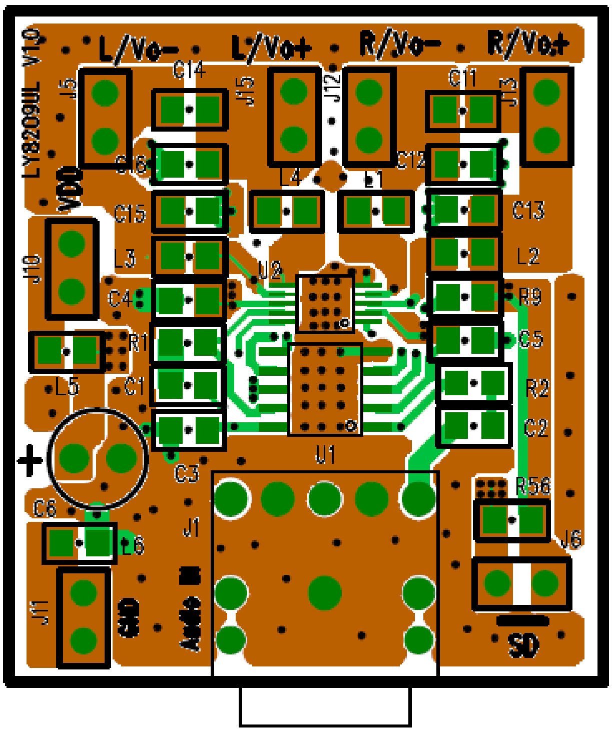
Top Silkscreen



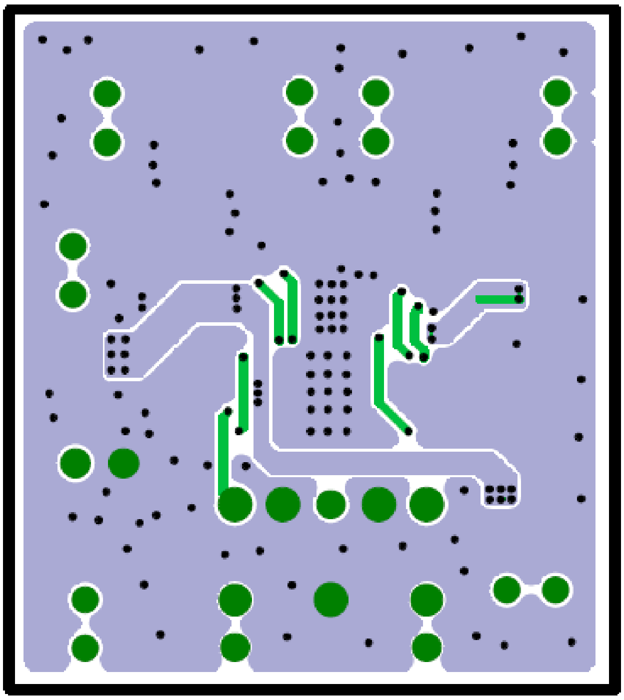
Top Layer



Composite view

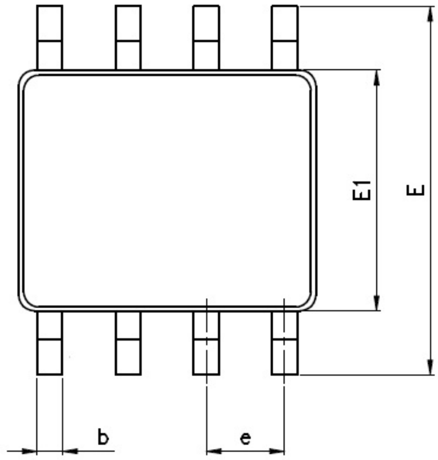


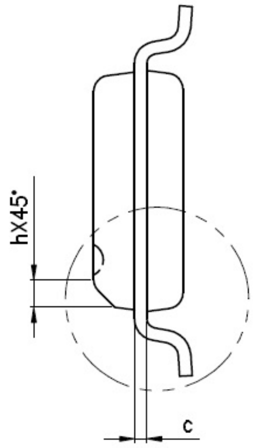
Bottom Layer

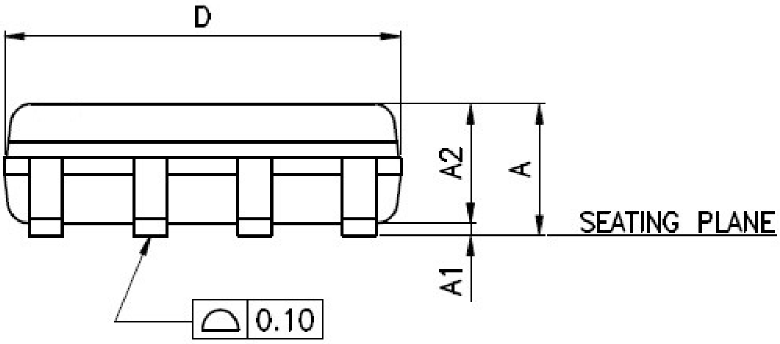


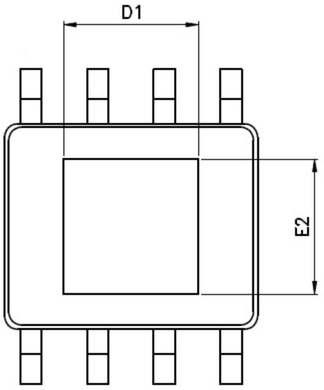
PACKAGE OUTLINE DIMENSION

8 Pin ESOP (150mil) Package Outline Dimension

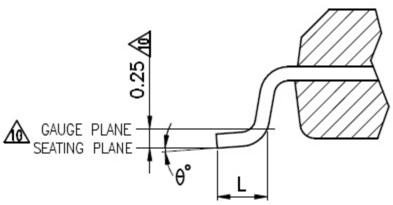








(THERMAL VARIATIONS ONLY)



Symbol	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.750	-	-	0.069
A1	0.00	-	0.25	0.000	-	0.0098
A2	1.24	-	-	0.049	-	-
b	0.31	-	0.51	0.012	-	0.020
c	0.1	-	0.25	0.004	-	0.010
D	4.90 BSC			0.19 BSC		
E	6.00 BSC			0.24 BSC		
E1	3.90 BSC			0.15 BSC		
e	1.27 BSC			0.05 BSC		
L	0.4	-	1.27	0.016	-	0.050
h	0.25	-	0.5	0.010	-	0.020
Θ˚	0	-	8	0	-	8
E2	2.05	-	2.513	0.081	-	0.099
D1	2.81	-	3.402	0.111	-	0.134

NOTES:
1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
MS-012 BA REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

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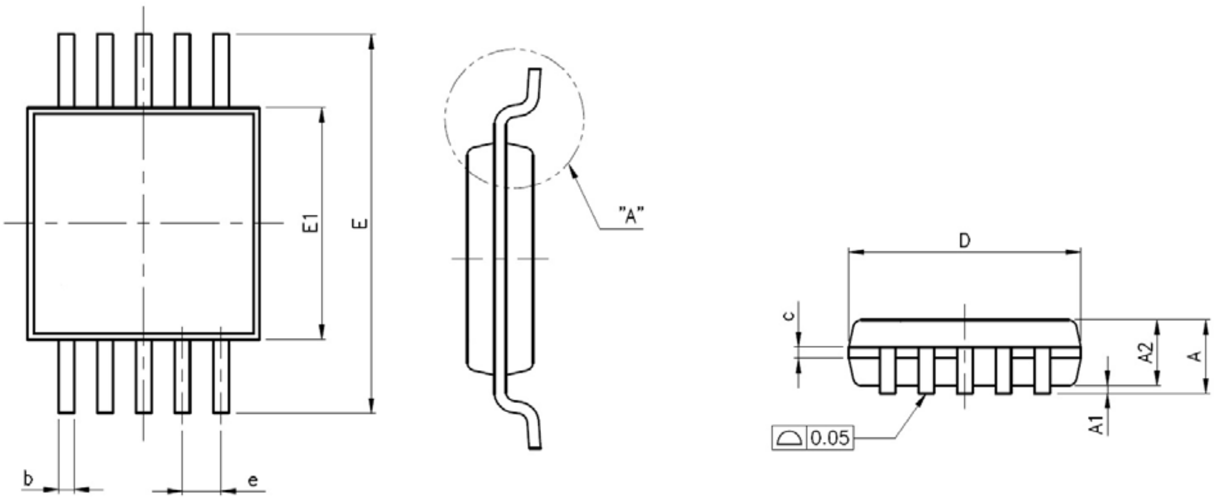
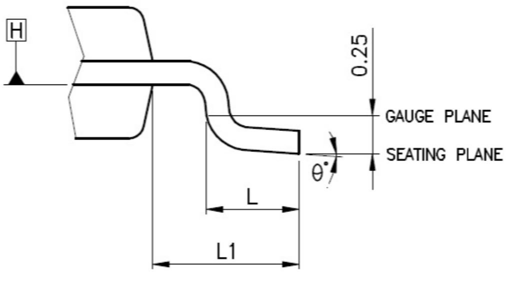
PACKAGE OUTLINE DIMENSION

10 Pin MSOP (118mil) Package Outline Dimension



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
b	0.17	–	0.27
c	0.08	–	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
θ°	0	–	8

UNIT : MM



DETAIL A

NOTES:
1.JEDEC OUTLINE :
STANDARD : MO–187 BA.
THERMALLY ENHANCED : MO–187 BA–T.
2.DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.
DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE.
3.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
4.D AND E1 DIMENSIONS ARE DETERMINED AT DATUM $\boxed{H}$.