REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Aug.12.2007
Rev. 1.1	Revised **TEST CONDITION** of I_{CC} Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS** Added packing type in **ORDERING INFORMATION**	Apr. 17.2009
Rev.1.2	Revised **ORDERING INFORMATION** in page 11	Aug.30.2010
Rev.1.3	Revised **GENERAL DESCRIPTION** & **PIN DESCRIPTION** in page 1 Revised I_{SB1} & I_{CC} in **FEATURES** & **PRODUCT FAMILY** Deleted -15ns Spec. Deleted **WRITE CYCLE** Notes : 1. WE#,CE#, LB#, UB# must be high during all address transitions. In page 7	Dec.14.2016

Lyontek Inc.

LY6112816

Rev. 1.3

5V 128K X 16 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 20ns
- Low power consumption:
  Operating current : 80mA(TYP.)
  Standby current :
  0.1mA (TYP.)
  20µA (TYP. for LL version)
- Single 5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP II

GENERAL DESCRIPTION

The LY6112816 is a 2,097,152-bit low power CMOS static random access memory organized as 131,072 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

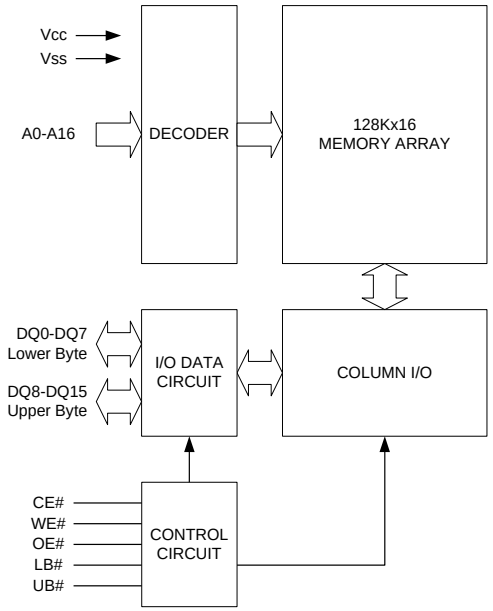
The LY6112816 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY6112816 operates from a single power supply of 5V and all outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
LY6112816	0 ~ 70℃	4.5 ~ 5.5V	20ns	0.1mA	80mA
LY6112816(E)	-20 ~ 80℃	4.5 ~ 5.5V	20ns	0.1mA	80mA
LY6112816(I)	-40 ~ 85℃	4.5 ~ 5.5V	20ns	0.1mA	80mA
LY6112816(LL)	0 ~ 70℃	4.5 ~ 5.5V	20ns	20µA	80mA
LY6112816(LLE)	-20 ~ 80℃	4.5 ~ 5.5V	20ns	20µA	80mA
LY6112816(LLI)	-40 ~ 85℃	4.5 ~ 5.5V	20ns	20µA	80mA

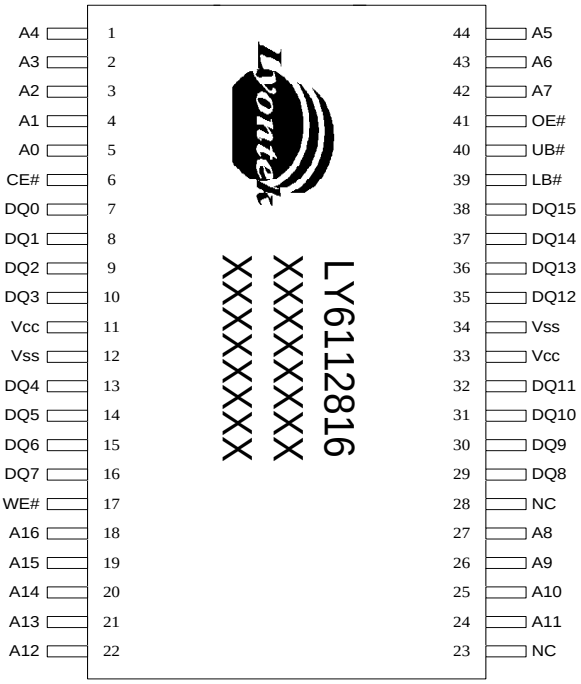
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION



TSOP II

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I_{SB1}
Output Disable	L	H	H	X	X	High-Z	High-Z	I_{CC}
	L	X	X	H	H	High-Z	High-Z	
Read	L	L	H	L	H	D_{OUT}	High-Z	I_{CC}
	L	L	H	H	L	High-Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High-Z	I_{CC}
	L	X	L	H	L	High-Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Input High Voltage	V_{IH} *1			0.6*V_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = MIN. CE# = V_{IL} , $I_{I/O}$ = 0mA Others at V_{IL} or V_{IH}		-	80	110	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq$ V_{CC} - 0.2V	Normal	-	0.1	3*5	mA
		Others at 0.2V or V_{CC}-0.2V	LL	-	20	100*6	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = $V_{CC(TYP.)}$ and T_A = 25℃
5. 1mA for special request
6. 50µA for special request

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -8mA/16mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY6112816-20		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	20		ns
Address Access Time	t_{AA}	-	20	ns
Chip Enable Access Time	t_{ACE}	-	20	ns
Output Enable Access Time	t_{OE}	-	8	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	4		ns
Output Enable to Output in Low-Z	t_{OLZ}*	0		ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	8	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	8	ns
Output Hold from Address Change	t_{OH}	3		ns
LB#, UB# Access Time	t_{BA}	-	8	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	8	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	4		ns

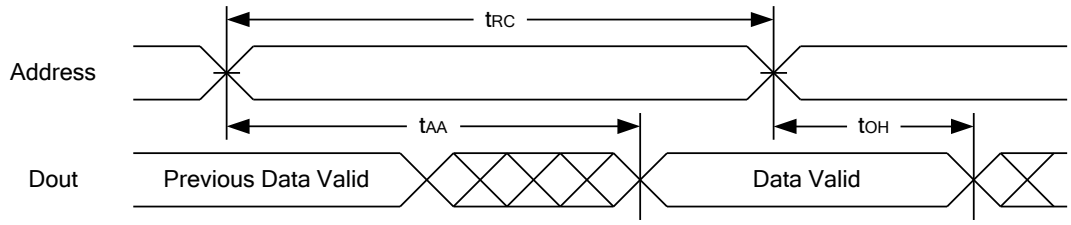
(2) WRITE CYCLE

PARAMETER	SYM.	LY6112816-20		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	20	-	ns
Address Valid to End of Write	t_{AW}	16	-	ns
Chip Enable to End of Write	t_{CW}	16	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	11	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	9	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	9	ns
LB#, UB# Valid to End of Write	t_{BW}	16	-	ns

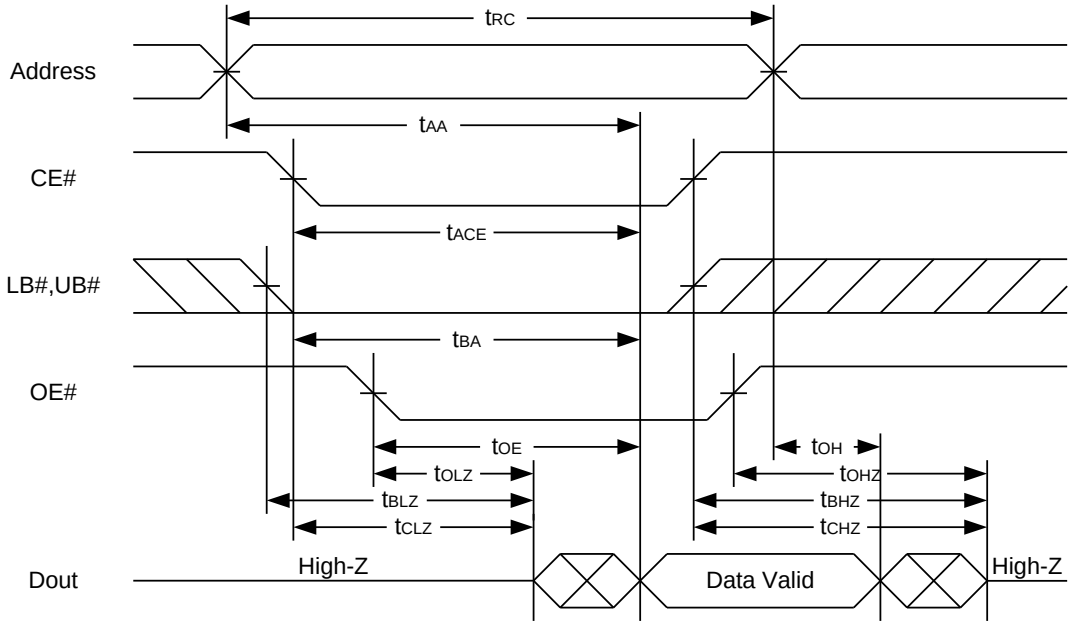
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

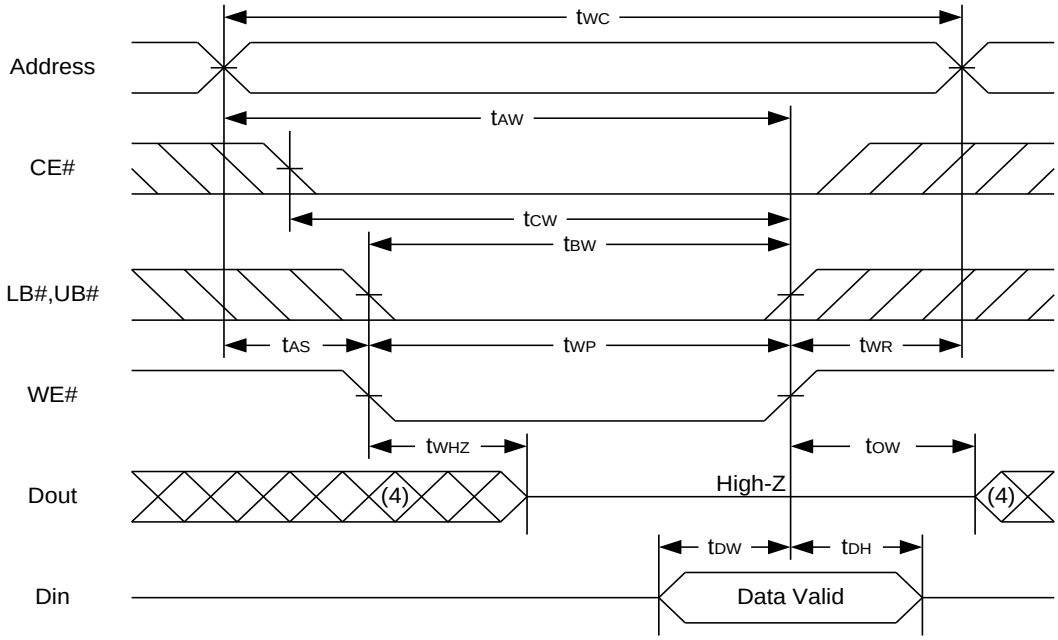


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

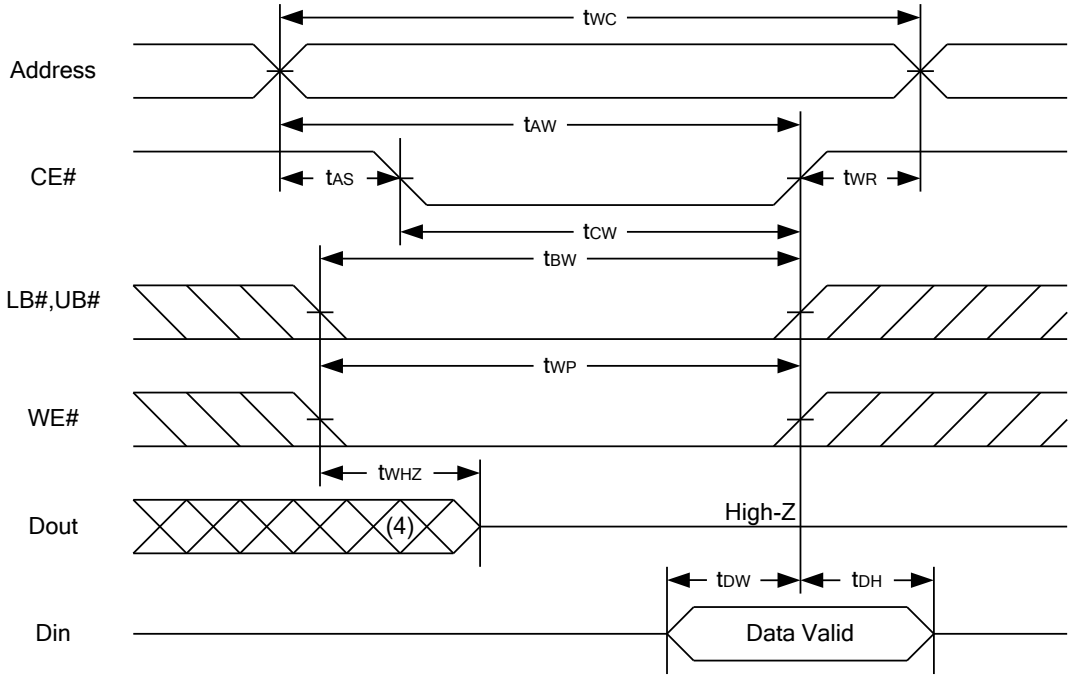


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3.Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

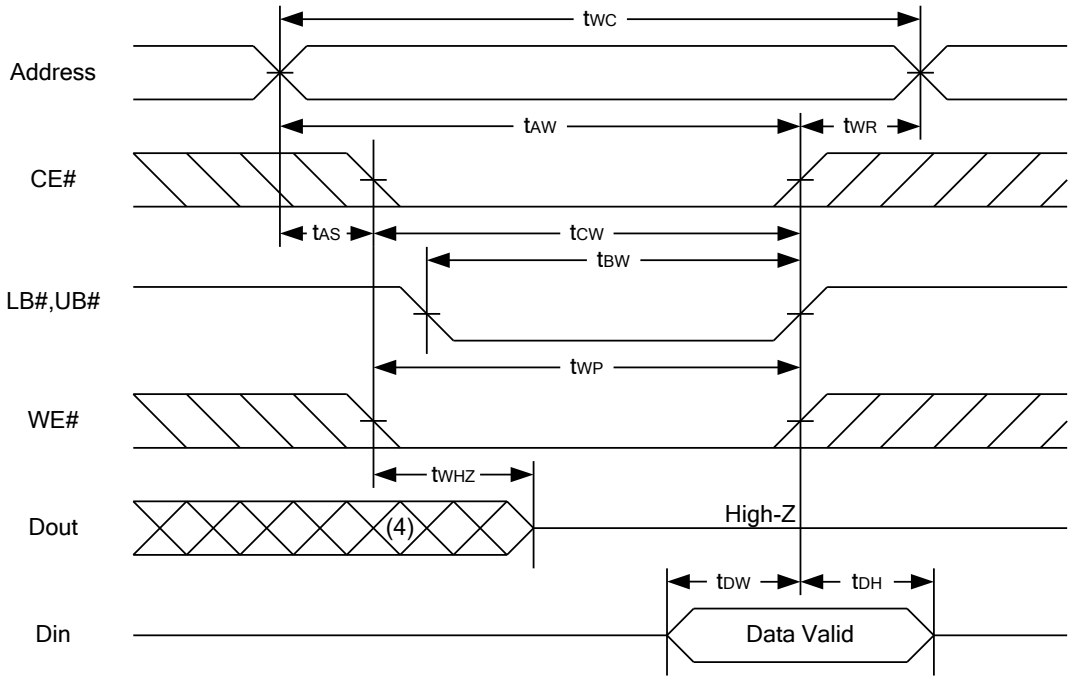
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



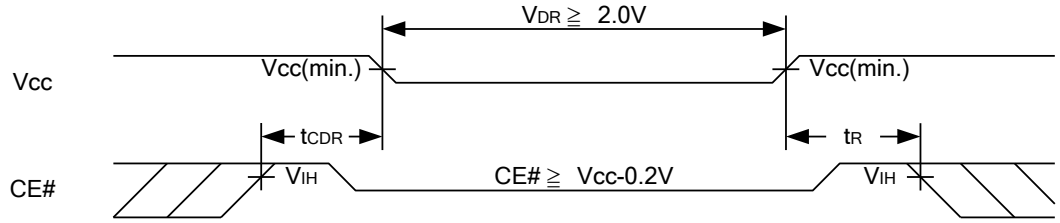
Notes :
1.A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3.During this period, I/O pins are in the output state, and input signals must not be applied.
4.If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V		2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V, CE# ≧ V_{CC} - 0.2V Other pins at 0.2V or V_{CC}-0.2V	Normal	-	0.05	2	mA
			LL	-	10	50	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC}*	-	-	ns

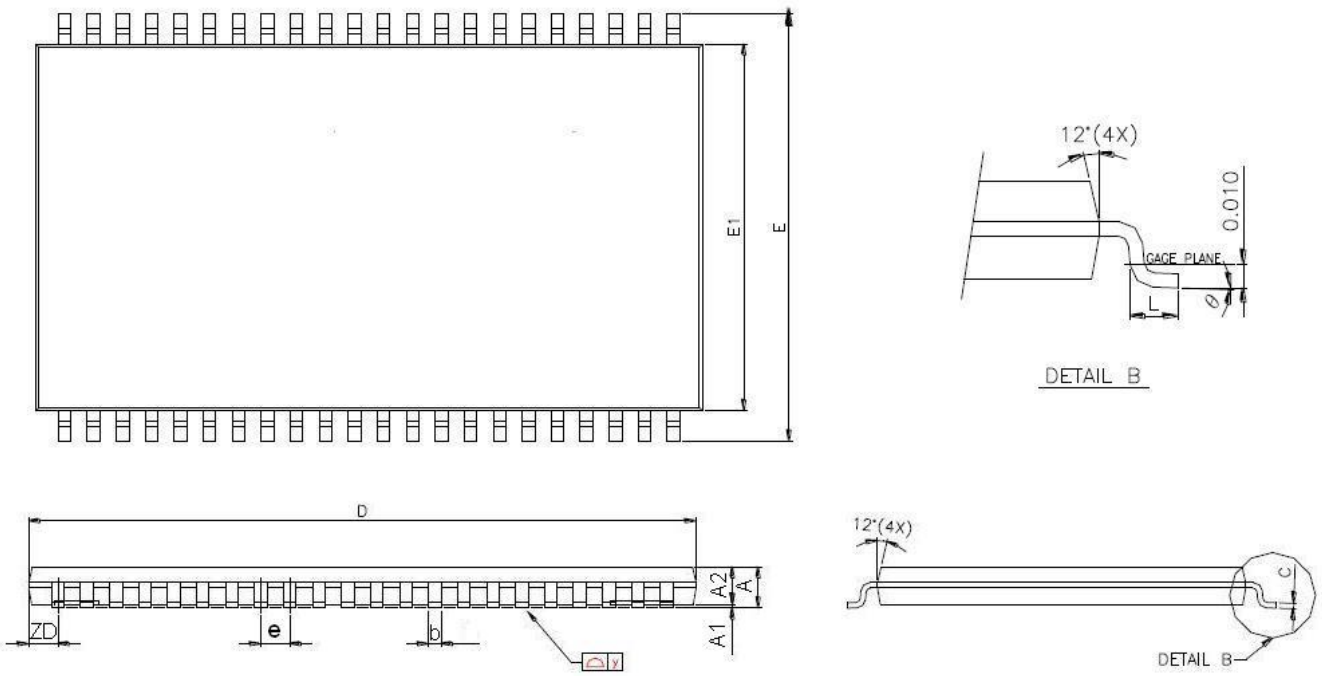
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP Ⅱ Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
44-pin (400mil) TSOP II	20	Normal Power	0℃~70℃	Tray	LY6112816ML-20
				Tape Reel	LY6112816ML-20T
			-20℃~80℃	Tray	LY6112816ML-20E
				Tape Reel	LY6112816ML-20ET
			-40℃~85℃	Tray	LY6112816ML-20I
				Tape Reel	LY6112816ML-20IT
		Ultra Low Power	0℃~70℃	Tray	LY6112816ML-20LL
				Tape Reel	LY6112816ML-20LLT
			-20℃~80℃	Tray	LY6112816ML-20LLE
				Tape Reel	LY6112816ML-20LLET
			-40℃~85℃	Tray	LY6112816ML-20LLI
				Tape Reel	LY6112816ML-20LLIT

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