REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issued	Feb.05. 2014
Rev. 1.1	Added LY61L102516AGL	Mar.26. 2014
Rev. 1.2	Revised I_{OH}/I_{OL} = -8mA/4mA to I_{OH}/I_{OL} = -4mA/8mA in **AC TEST CONDITIONS**	Sep.04. 2014
Rev. 1.3	Added V_{CC}=1.8V specifications Revised **PIN DESCRIPTION** in page 1 Deleted **WRITE CYCLE** Notes : 1. WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions. in page 10	Aug.16.2017
Rev. 1.4	Revised **TEST CONDITION** of I_{CC1} in page 4 Revised **TIMING WAVEFORMS** of **WRITE CYCLE** in page 9 & 10	Mar.03.2020

Lyontek Inc.

LY61L102516A

Rev. 1.4

1024K X 16 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10ns (V_{CC}=3.3V)
  15ns (V_{CC}=1.8V)
- **Low power consumption:**
  Operating current:
  70mA (3.3V TYP.)
  50mA (1.8V TYP.)
  Standby current : 4mA(TYP.)
- Power supply: 1.8 or 3.3V
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 54-pin 400mil TSOP II
  48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

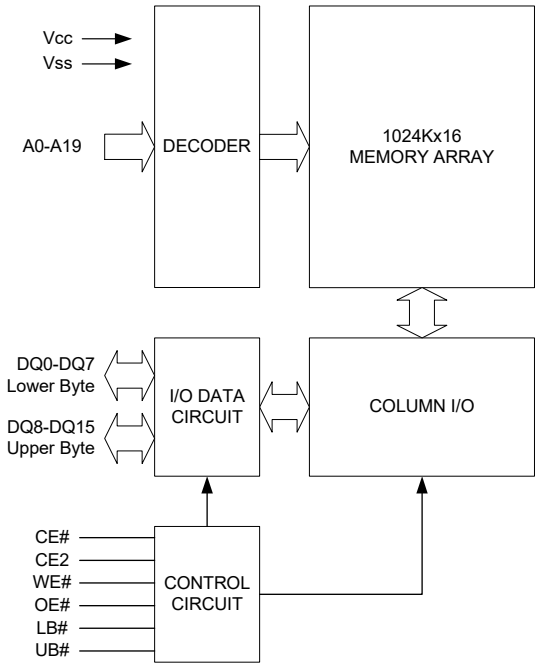
The LY61L102516A is a 16M-bit high speed CMOS static random access memory organized as 1024K words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY61L102516A operates power supply either 1.8V or 3.3V, and all inputs and outputs are fully TTL compatible.

PRODUCT FAMILY

Product Family	Operating Temp.	Speed		Power Dissipation			
				Standby (I_{SB1}, TYP.)		Operating (I_{CC1}, TYP.)	
		V_{CC}=1.65~2.4V	V_{CC}=2.7 ~3.6V	V_{CC}=1.65~2.4V	V_{CC}=2.7 ~3.6V	V_{CC}=1.65~2.4V	V_{CC}=2.7 ~3.6V
LY61L102516A	0 ~ 70℃	15ns	10ns	4mA	4mA	50mA	70mA
LY61L102516A(I)	-40 ~ 85℃	15ns	10ns	4mA	4mA	50mA	70mA

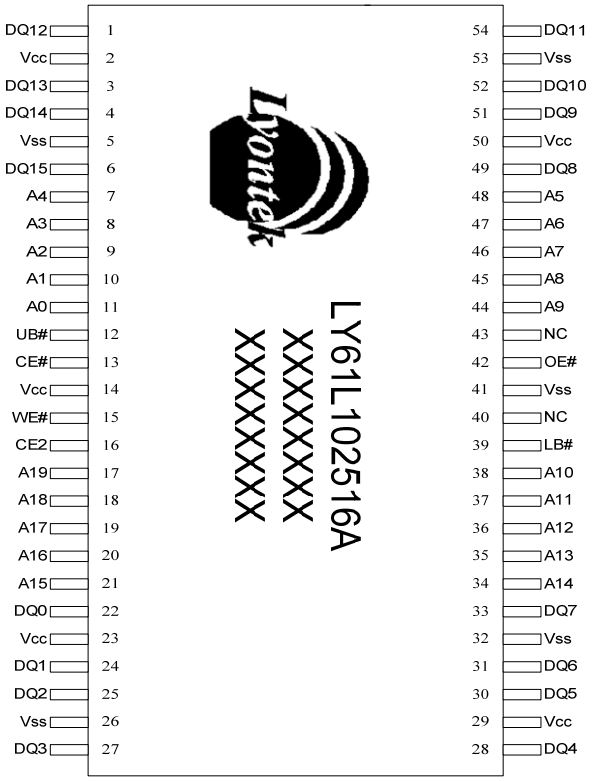
FUNCTIONAL BLOCK DIAGRAM



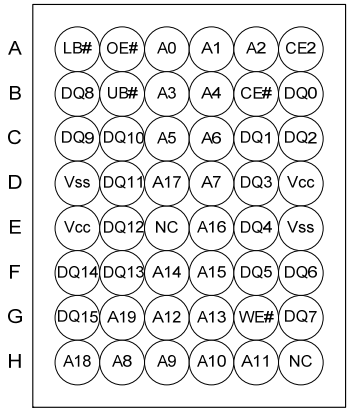
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION



TSOP II(Top View)



TFBGA(See through with Top View)

TFBGA

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade) -40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0 - DQ7	DQ8 - DQ15	
Standby	H X	X L	X X	X X	X X	X X	High-Z High-Z	High-Z High-Z	I_{SB1}
Output Disable	L L	H H	H H	H H	L X	X L	High-Z High-Z	High-Z High-Z	I_{CC},I_{CC1}
Read	L L L	H H H	L L L	H H H	L H L	H L L	D_{OUT} High-Z D_{OUT}	High-Z D_{OUT} D_{OUT}	I_{CC},I_{CC1}
Write	L L L	H H H	X X X	L L L	L H L	H L L	D_{IN} High-Z D_{IN}	High-Z D_{IN} D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC}=2.7V~3.6V)

PARAMETER	SYM.	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.3	3.6	V
Input High Voltage	V_{IH} *1			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC1}	CE# ≤0.2V and CE2≧ V_{CC}-0.2V, other pins at 0.2V or V_{CC}-0.2V, $I_{I/O}$ = 0mA; f=MAX.	-10	-	70	120	mA
			-12	-	65	110	mA
Standby Power Supply Current	I_{SB1}	CE# ≧ V_{CC} - 0.2V; Other pins at 0.2V or V_{CC}-0.2V.		-	4	40	mA

Notes:
1. V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

DC ELECTRICAL CHARACTERISTICS (V_{CC}=1.65V~2.4V)

PARAMETER	SYM.	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			1.65	1.8	2.4	V
Input High Voltage	V_{IH} *1			1.4	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			- 0.3	-	0.4	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA		1.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC1}	CE# ≤0.2V and CE2≧ V_{CC}-0.2V, other pins at 0.2V or V_{CC}-0.2V, $I_{I/O}$ = 0mA; f=MAX.	-15	-	50	90	mA
Standby Power Supply Current	I_{SB1}	CE# ≧ V_{CC} - 0.2V; Other pins at 0.2V or V_{CC}-0.2V.		-	4	40	mA

Notes:
1. V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	10ns(V_{CC}=3.3V), 15ns(V_{CC}=1.8V)
Input Pulse Levels	0.2V to V_{CC}-0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	V_{CC}/2
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -4mA/8mA(V_{CC}=3.3V) I_{OH}/I_{OL} = -0.5mA/1mA(V_{CC}=1.8V)

AC ELECTRICAL CHARACTERISTICS (V_{CC}=2.7V~3.6V)

(1) READ CYCLE

PARAMETER	SYM.	LY61L102516A-10		LY61L102516A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	ns
Address Access Time	t_{AA}	-	10	-	12	ns
Chip Enable Access Time	t_{ACE}	-	10	-	12	ns
Output Enable Access Time	t_{OE}	-	4.5	-	5	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	2	-	3	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	4	-	5	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	4	-	5	ns
Output Hold from Address Change	t_{OH}	2	-	2	-	ns
LB#, UB# Access Time	t_{BA}	-	4.5	-	5	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	4	-	5	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	0	-	0	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	LY61L102516A-10		LY61L102516A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	ns
Chip Enable to End of Write	t_{CW}	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	2	-	2	-	ns
Write to Output in High-Z	t_{WHZ}*	-	4	-	5	ns
LB#, UB# Valid to End of Write	t_{BW}	8	-	10	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC}=1.65V~2.4V)

(1) READ CYCLE

PARAMETER	SYM.	LY61L102516A-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	15	-	ns
Address Access Time	t_{AA}	-	15	ns
Chip Enable Access Time	t_{ACE}	-	15	ns
Output Enable Access Time	t_{OE}	-	8	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	3	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	5	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	5	ns
Output Hold from Address Change	t_{OH}	2	-	ns
LB#, UB# Access Time	t_{BA}	-	8	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	5	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	0	-	ns

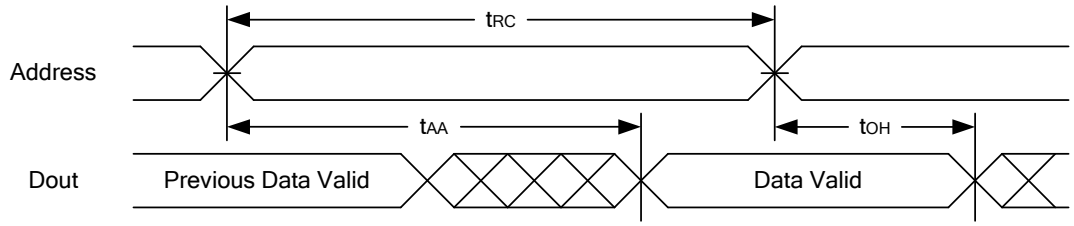
(2) WRITE CYCLE

PARAMETER	SYM.	LY61L102516A-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	15	-	ns
Address Valid to End of Write	t_{AW}	12	-	ns
Chip Enable to End of Write	t_{CW}	12	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	12	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	9	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	2	-	ns
Write to Output in High-Z	t_{WHZ}*	-	9	ns
LB#, UB# Valid to End of Write	t_{BW}	12	-	ns

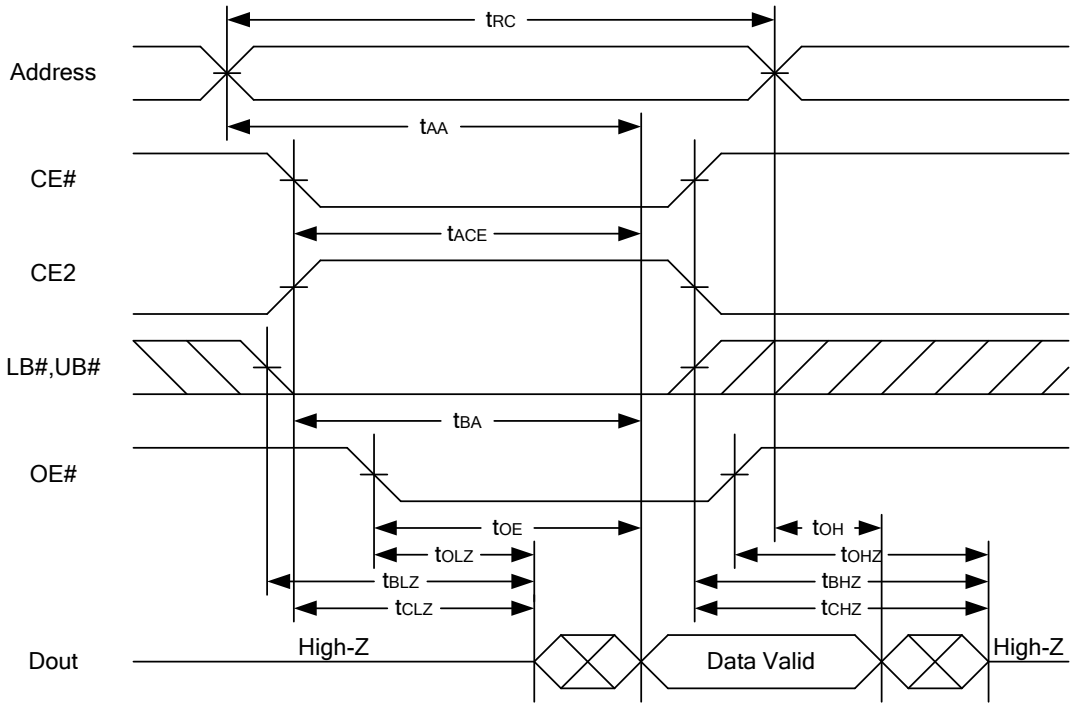
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

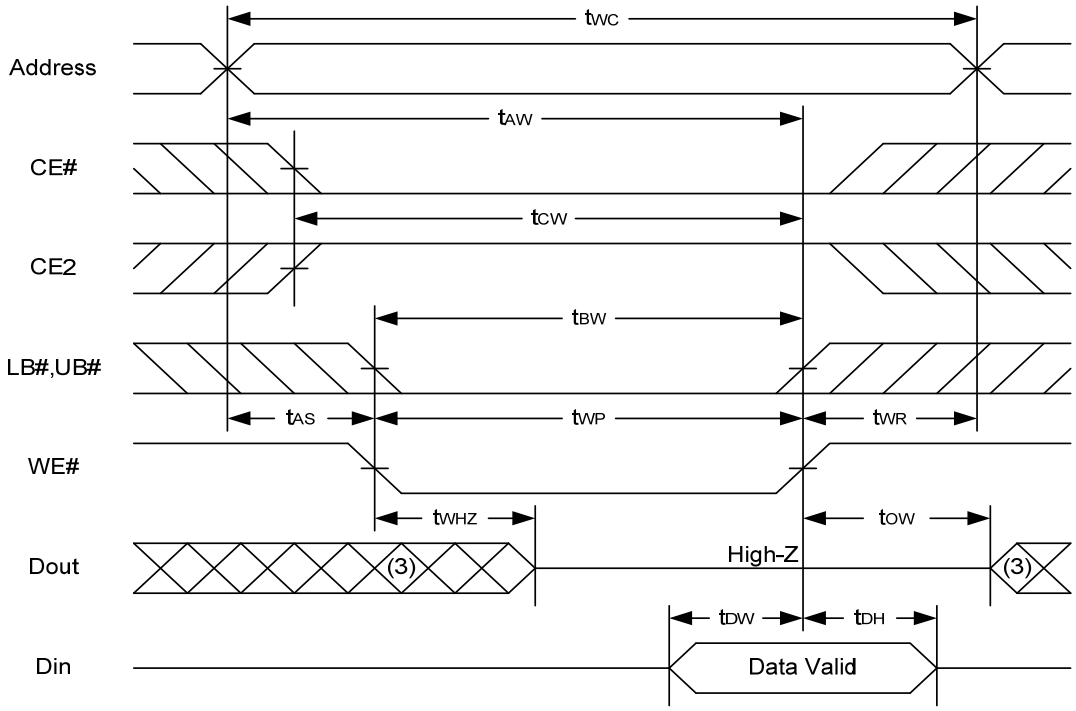


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

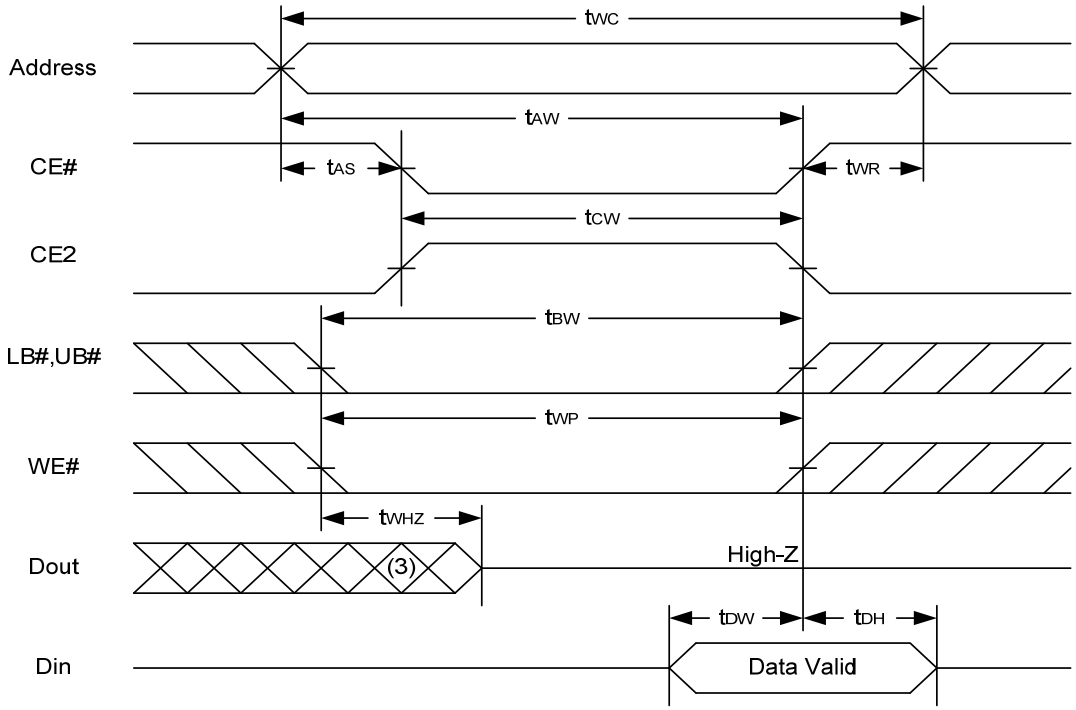


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

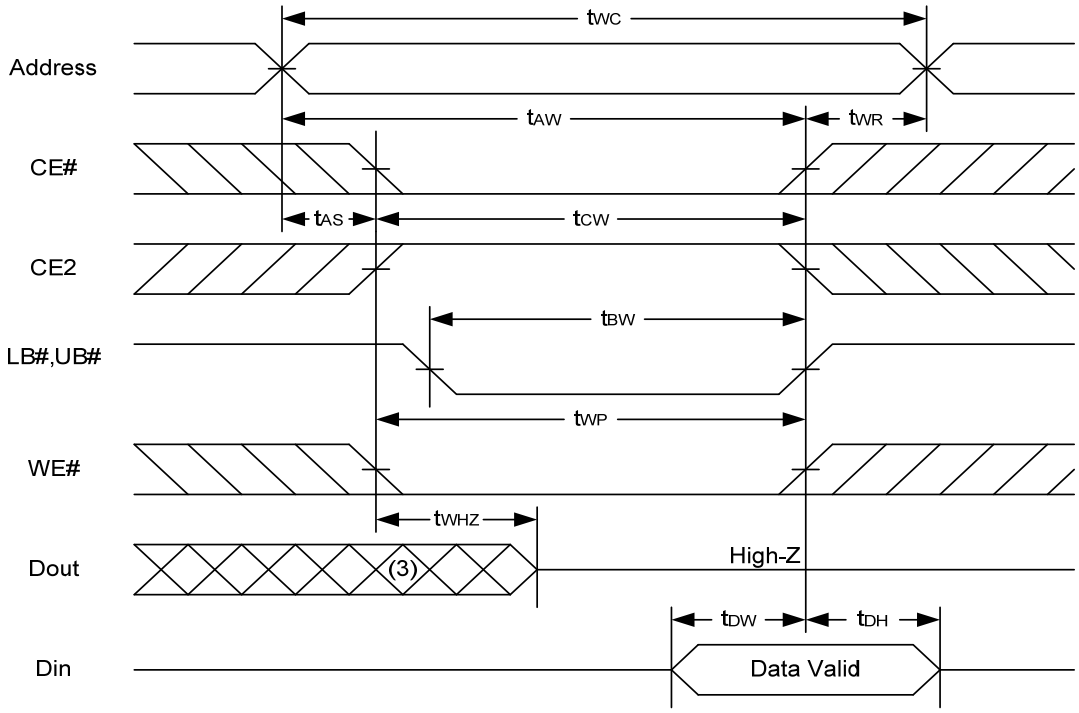
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :
1.A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
3.During this period, I/O pins are in the output state, and input signals must not be applied.
4.If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

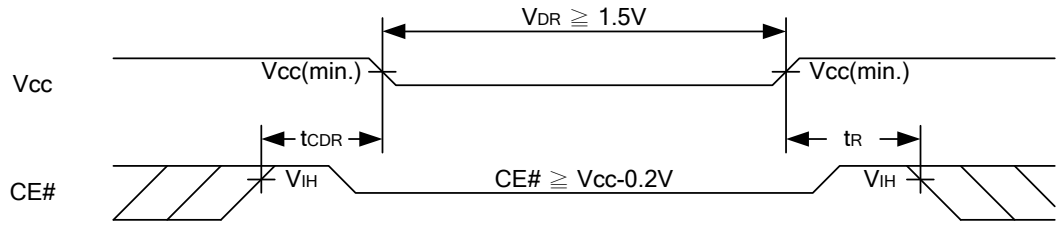
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V Other pins at 0.2V or V_{CC}-0.2V	-	4	40	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

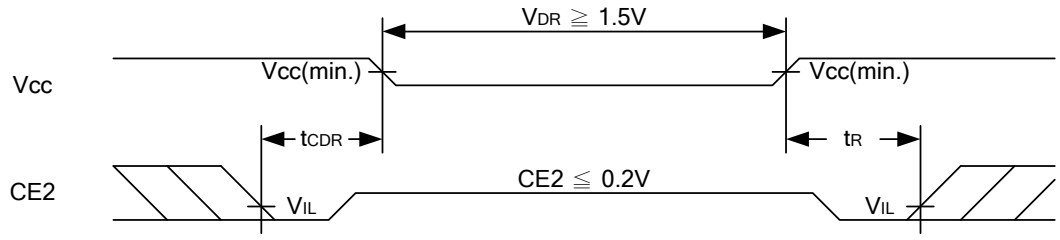
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

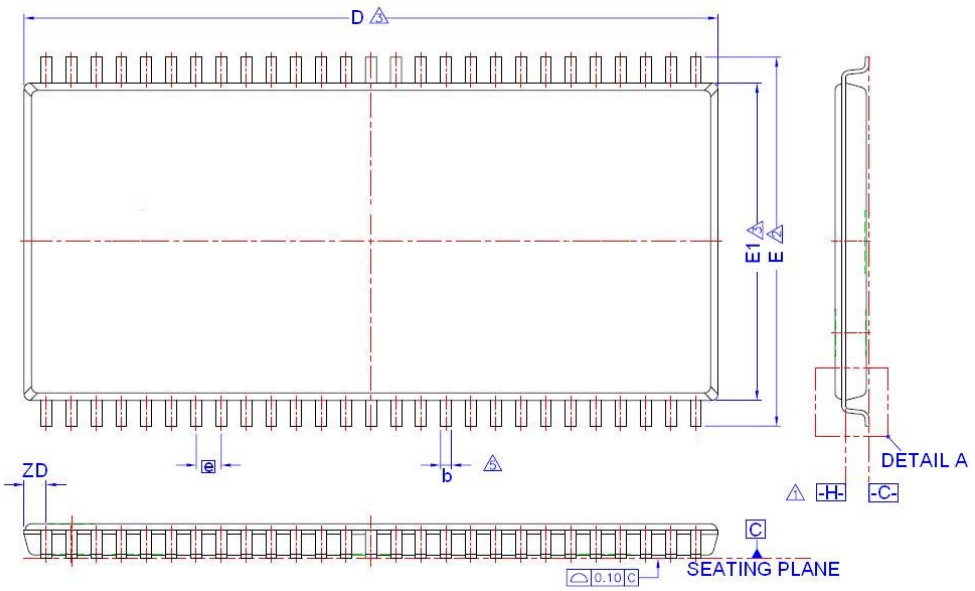


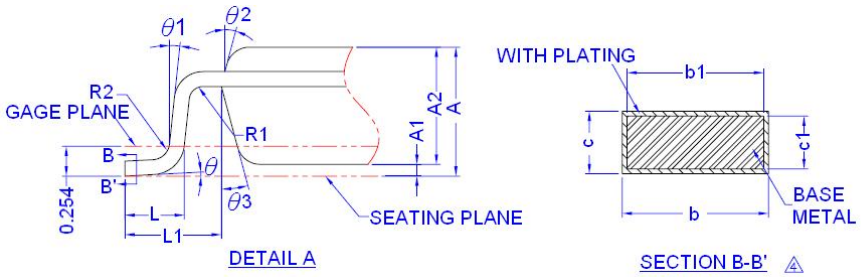
Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

54-pin 400 mil TSOP II Package Outline Dimension

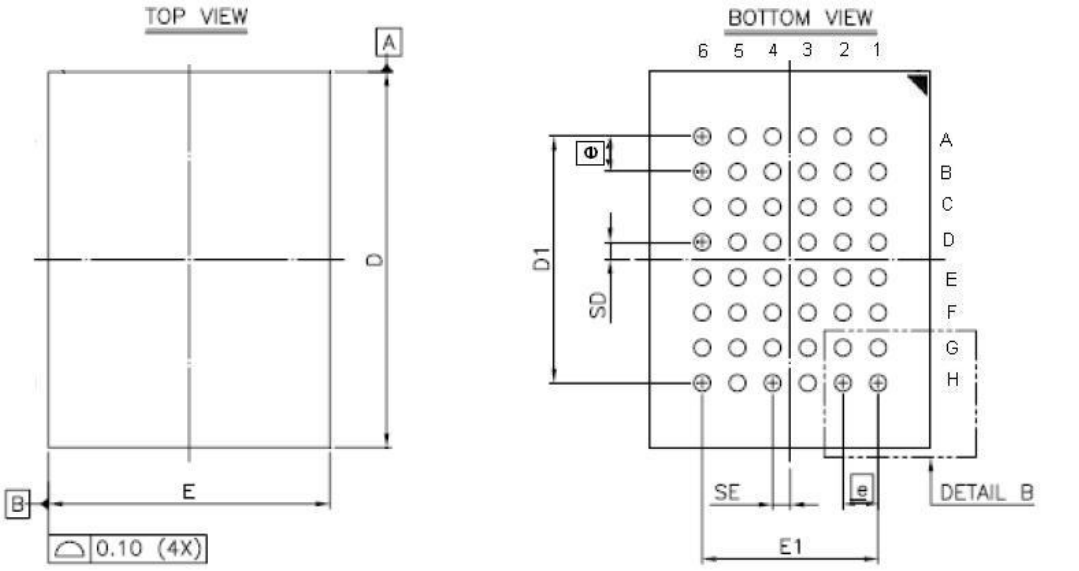


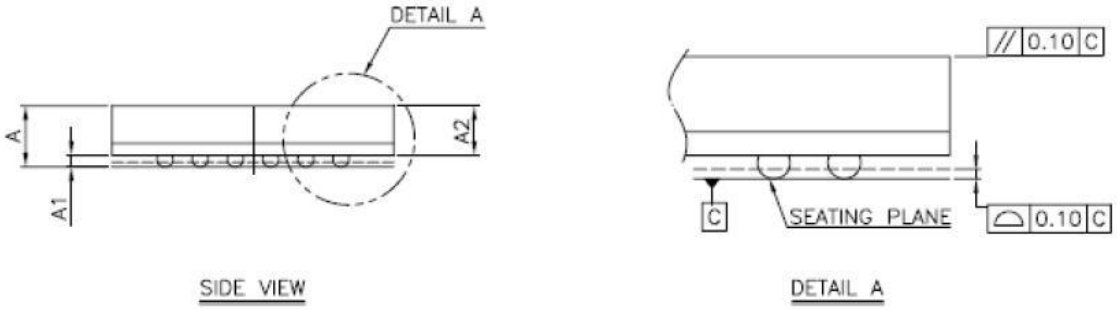


SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	–	0.45	0.012	–	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	–	0.21	0.005	–	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.71 REF			0.028 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
R1	0.12	–	–	0.005	–	–
R2	0.12	–	0.25	0.005	–	0.010
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–
θ2	10°	15°	20°	10°	15°	20°
θ3	10°	15°	20°	10°	15°	20°

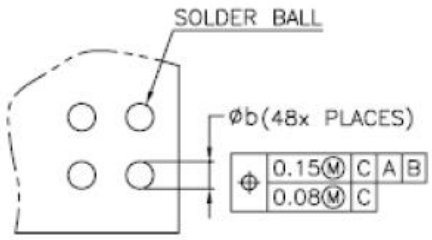
NOTE:
1. DATUM PLANE -H- COINCIDENT WITH BOTTOM OF LEAD. WHERE LEAD EXITS BODY.
2. TO BE DETERMINED AT SEATING PLANE -C- .
3. DIMENSION D AND E1 ARE DETERMINED AT DATUM -H- .
   DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. REFER TO JEDEC STD MS-024, FA.

48-ball 6mm × 8mm TFBGA Package Outline Dimension





SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		



NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(℃)	Packing Type	Lyontek Item No.
54-pin (400mil) TSOP II	10	0℃~70℃	Tray	LY61L102516AML-10
			Tape Reel	LY61L102516AML-10T
		-40℃~85℃	Tray	LY61L102516AML-10I
			Tape Reel	LY61L102516AML-10IT

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(℃)	Packing Type	Lyontek Item No.
48-ball (6mm x 8mm) TFBGA	10	0℃~70℃	Tray	LY61L102516AGL-10
			Tape Reel	LY61L102516AGL-10T
		-40℃~85℃	Tray	LY61L102516AGL-10I
			Tape Reel	LY61L102516AGL-10IT

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