

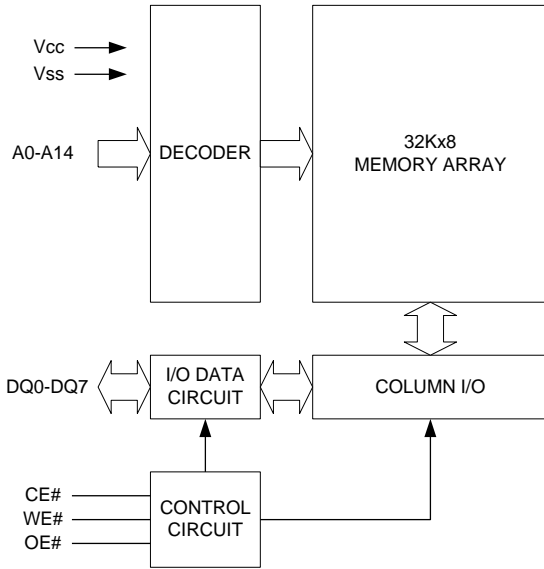


#### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Revised $V_{TERM}$ to $V_{T1}$ and $V_{T2}$ Revised <b>TEST CONDITION</b> of $I_{SB1}/I_{DR}$ Added LL Spec.	Feb.02.2009
Rev. 1.2	Revised <b>TEST CONDITION</b> of $I_{CC}/I_{SB}$ Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b>Lead free and green package available to Green package available</b> Deleted $T_{SOLDER}$ in <b>ABSOLUTE MAXIMUM RATINGS</b> Added packing type in <b>ORDERING INFORMATION</b>	Apr.17.2009
Rev. 1.3	Revised <b>PACKAGE OUTLINE DIMENSION</b> in page 8	May.07.2010
Rev. 1.4	Revised <b>ORDERING INFORMATION</b> in page 10	Aug.31.2010
Rev. 1.5	Revised <b>ORDERING INFORMATION</b> in page 11	Jan.06.2015
Rev. 1.6	Deleted -10ns Spec. Deleted <b>WRITE CYCLE</b> Notes : 1. WE#, CE# must be high during all address transitions. in page 7.	May.10.2017



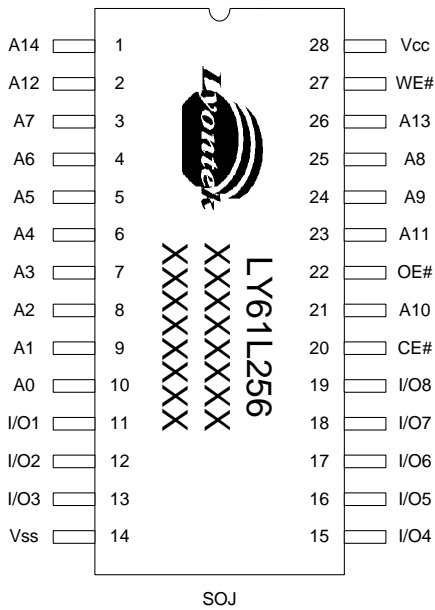
### FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

### PIN CONFIGURATION





### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to V <sub>SS</sub>	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

### TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*4	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		-12/-15	3.0	3.3	3.6	V
Input High Voltage	V <sub>IH</sub> *1			2.0	-	V <sub>CC</sub> +0.5	V
Input Low Voltage	V <sub>IL</sub> *2			- 0.5	-	0.6	V
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>		- 1	-	1	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled		- 1	-	1	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA		2.4	3.0	-	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA		-	-	0.4	V
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = MIN. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Others at V <sub>IL</sub> or V <sub>IH</sub>	-12	-	50	60	mA
			-15	-	40	50	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> -0.2V		-	1	5	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# = V <sub>IH</sub> , others at V <sub>IL</sub> or V <sub>IH</sub>		-	10	15	mA
		CE# ≥ V <sub>CC</sub> - 0.2V	Normal	-	0.5	3	mA
		CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> -0.2V	LL	-	1	20	μA

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -4mA/8mA

**AC ELECTRICAL CHARACTERISTICS**
**(1) READ CYCLE**

PARAMETER	SYM.	LY61L256-12		LY61L256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	12	-	15	-	ns
Address Access Time	t <sub>AA</sub>	-	12	-	15	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	12	-	15	ns
Output Enable Access Time	t <sub>OE</sub>	-	6	-	7	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	3	-	4	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	0	-	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	6	-	7	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	6	-	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	ns

**(2) WRITE CYCLE**

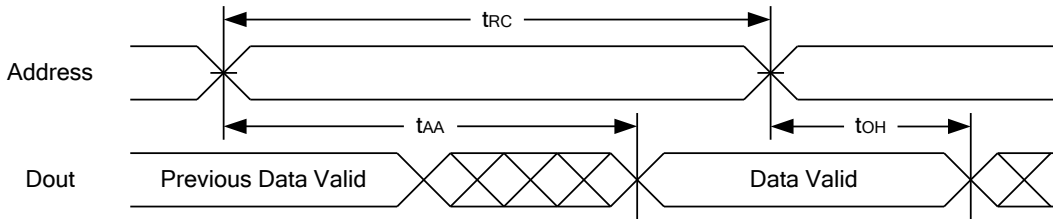
PARAMETER	SYM.	LY61L256-12		LY61L256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	12	-	15	-	ns
Address Valid to End of Write	t <sub>AW</sub>	10	-	12	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	10	-	12	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	9	-	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	7	-	8	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	3	-	4	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	7	-	8	ns

\*These parameters are guaranteed by device characterization, but not production tested.

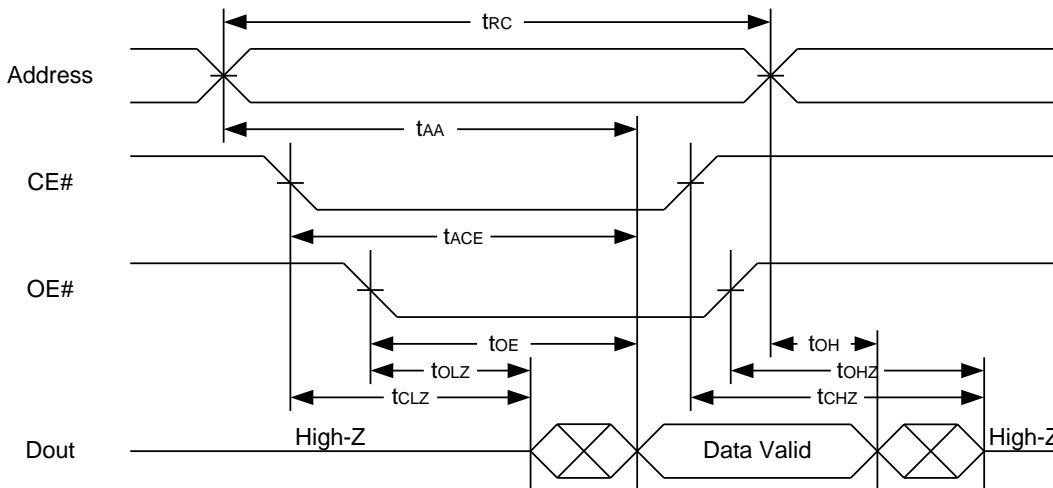


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



#### Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .





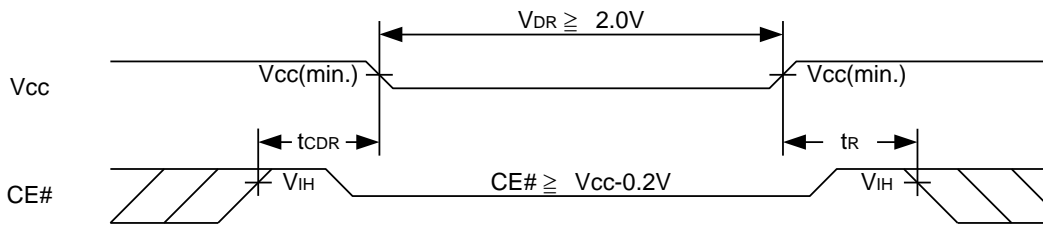


### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	2.0	-	3.6	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 2.0V CE# ≥ V <sub>CC</sub> - 0.2V	Normal	-	0.3	2	mA
		V <sub>CC</sub> = 2.0V, CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> -0.2V	LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns	

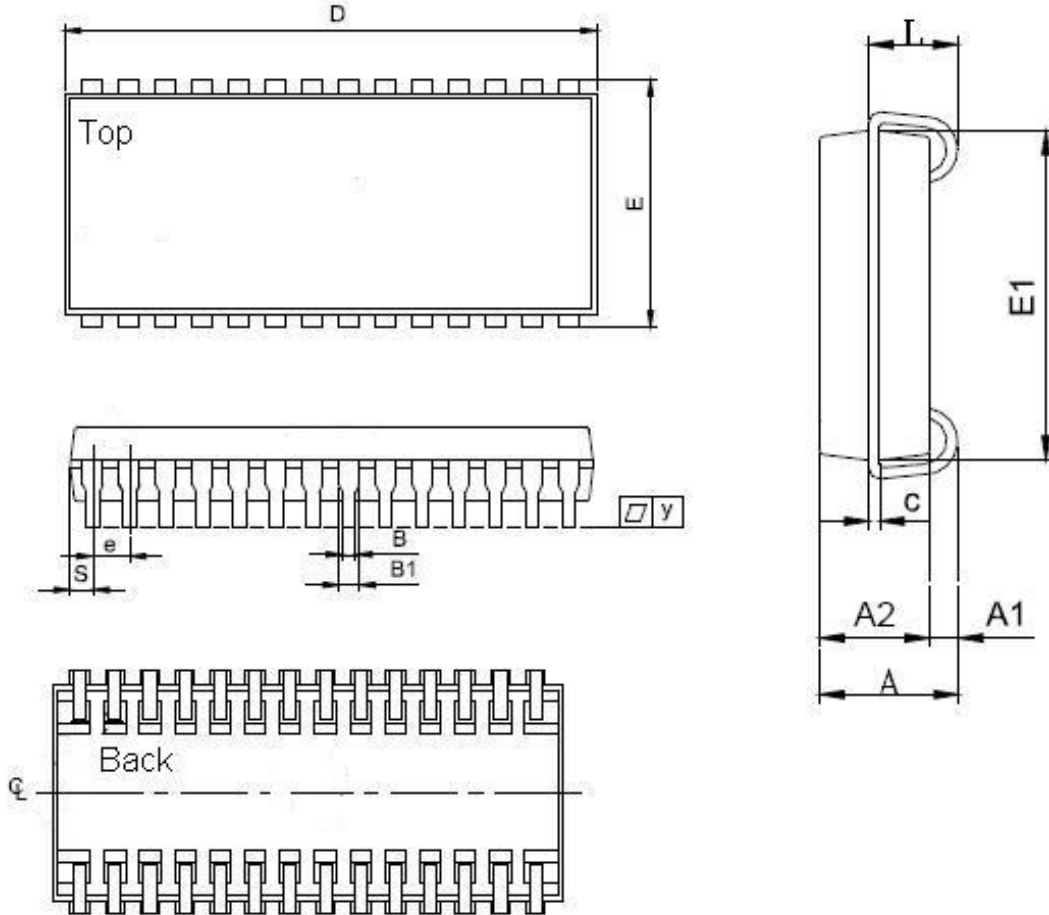
t<sub>RC</sub>\* = Read Cycle Time

### DATA RETENTION WAVEFORM



#### PACKAGE OUTLINE DIMENSION

28-pin 300 mil SOJ Package Outline Dimension



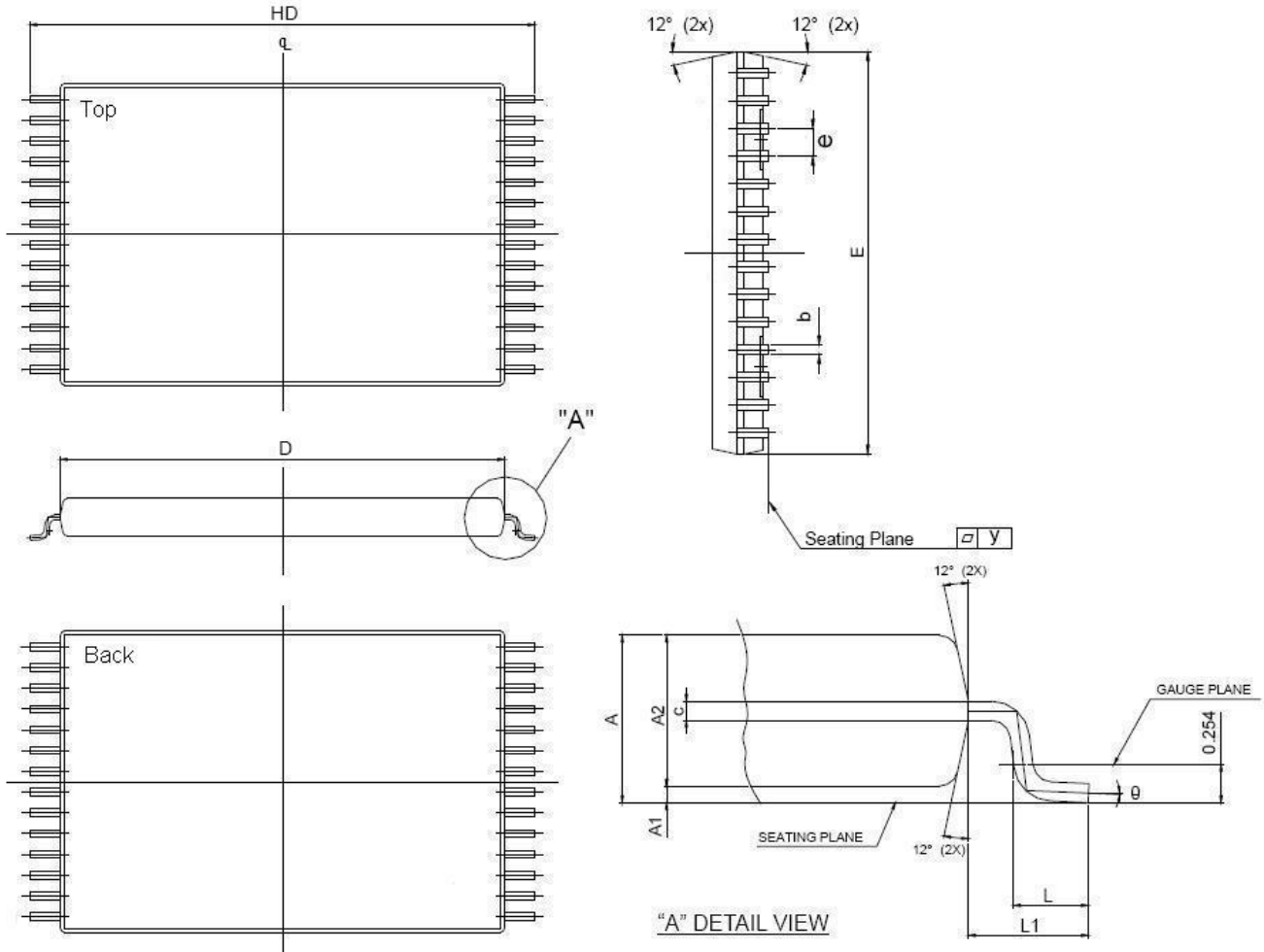
SYM.	UNIT	INCH(REF)	MM(BASE)
A		0.140(MAX)	3.556(MAX)
A1		0.025(MIN)	0.635(MIN)
A2		0.100±0.015	2.540±0.381
B		0.018±0.004	0.457±0.102
B1		0.028±0.004	0.711±0.102
c		0.010±0.004	0.254±0.102
D		0.710±0.020	18.03±0.508
E		0.337±0.010	8.560±0.254
E1		0.300±0.005	7.620±0.127
e		0.050±0.006	1.270±0.152
L		0.087±0.010	2.210±0.254
S		0.045(MAX)	1.143(MAX)
Y		0.004(MAX)	0.102(MAX)

Note : 1.S/E/D dimension is not including mold flash.

2.The end flash in package lengthwise is not more than 10 mils each side.



**28-pin 8 x 13.4mm sTSSOP Package Outline Dimension**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin (300mil) SOJ	12	Normal Power	0°C~70°C	Tube	LY61L256JL-12
				Tape Reel	LY61L256JL-12T
			-20°C~80°C	Tube	LY61L256JL-12E
				Tape Reel	LY61L256JL-12ET
			-40°C~85°C	Tube	LY61L256JL-12I
				Tape Reel	LY61L256JL-12IT
	15	Normal Power	0°C~70°C	Tube	LY61L256JL-15
				Tape Reel	LY61L256JL-15T
			-20°C~80°C	Tube	LY61L256JL-15E
				Tape Reel	LY61L256JL-15ET
			-40°C~85°C	Tube	LY61L256JL-15I
				Tape Reel	LY61L256JL-15IT
	12	Ultra Low Power	0°C~70°C	Tube	LY61L256JL-12LL
				Tape Reel	LY61L256JL-12LLT
			-20°C~80°C	Tube	LY61L256JL-12LLE
				Tape Reel	LY61L256JL-12LLET
			-40°C~85°C	Tube	LY61L256JL-12LLI
				Tape Reel	LY61L256JL-12LLIT
	15	Ultra Low Power	0°C~70°C	Tube	LY61L256JL-15LL
				Tape Reel	LY61L256JL-15LLT
-20°C~80°C			Tube	LY61L256JL-15LLE	
			Tape Reel	LY61L256JL-15LLET	
-40°C~85°C			Tube	LY61L256JL-15LLI	
			Tape Reel	LY61L256JL-15LLIT	



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin (8mm x 13.4mm) sTSOP	12	Normal Power	0°C~70°C	Tray	LY61L256RL-12
				Tape Reel	LY61L256RL-12T
			-20°C~80°C	Tray	LY61L256RL-12E
				Tape Reel	LY61L256RL-12ET
			-40°C~85°C	Tray	LY61L256RL-12I
				Tape Reel	LY61L256RL-12IT
	15	Normal Power	0°C~70°C	Tray	LY61L256RL-15
				Tape Reel	LY61L256RL-15T
			-20°C~80°C	Tray	LY61L256RL-15E
				Tape Reel	LY61L256RL-15ET
			-40°C~85°C	Tray	LY61L256RL-15I
				Tape Reel	LY61L256RL-15IT
	12	Ultra Low Power	0°C~70°C	Tray	LY61L256RL-12LL
				Tape Reel	LY61L256RL-12LLT
			-20°C~80°C	Tray	LY61L256RL-12LLE
				Tape Reel	LY61L256RL-12LLET
			-40°C~85°C	Tray	LY61L256RL-12LLI
				Tape Reel	LY61L256RL-12LLIT
	15	Ultra Low Power	0°C~70°C	Tray	LY61L256RL-15LL
				Tape Reel	LY61L256RL-15LLT
-20°C~80°C			Tray	LY61L256RL-15LLE	
			Tape Reel	LY61L256RL-15LLET	
-40°C~85°C			Tray	LY61L256RL-15LLI	
			Tape Reel	LY61L256RL-15LLIT	



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