REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Aug.27.2010
Rev. 1.1	Delete **E-Grade,** revise **ordering information** in page 10.	Apr.06.2012
Rev. 1.2	Removed Package Type : SOJ	Apr. 08. 2019

Lyontek Inc.

LY65W64

Rev. 1.2

8K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 25ns
- Low power consumption:
  Operating current : 30mA (TYP.)
  Standby current : 1μA (TYP.)
- Single 3~5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- Green package available
- Package : 28-pin 8mm x 13.4mm sTSOP

GENERAL DESCRIPTION

The LY65W64 is a 65,536-bit high speed CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY65W64 is well designed for high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY65W64 operates from a single power supply of 3~5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(Icc,TYP.)
LY65W64(LL)	0 ~ 70℃	3.0 ~ 5.5V	25ns	1μA	30mA
LY65W64(LLI)	-40 ~ 85℃	3.0 ~ 5.5V	25ns	1μA	30mA

FUNCTIONAL BLOCK DIAGRAM
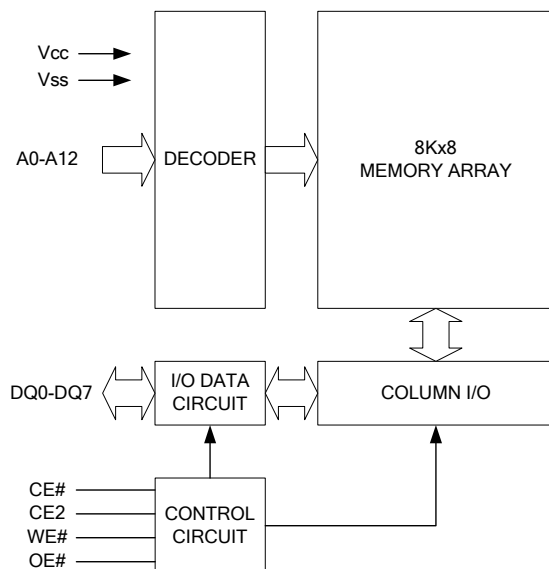
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION

OE#	1		28	A10
A11	2		27	CE#
A9	3		26	DQ7
A8	4		25	DQ6
CE2	5	LY65W64	24	DQ5
WE#	6	XXXXXXXX	23	DQ4
Vcc	7		22	DQ3
NC	8	XXXXXXXX	21	Vss
A12	9		20	DQ2
A7	10		19	DQ1
A6	11		18	DQ0
A5	12		17	A0
A4	13		16	A1
A3	14		15	A2

sTSOP

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB1}
	X	L	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. [*4]	MAX.	UNIT
Supply Voltage	V_{CC}		3.0	3.3	5.5	V
Input High Voltage	V_{IH}[*1]	V_{CC}=3.0~3.6V	2.0	-	V_{CC}+0.5	V
		V_{CC}=4.5~5.5V	2.4	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}[*2]	V_{CC}=3.0~3.6V	- 0.5	-	0.6	V
		V_{CC}=4.5~5.5V	- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geq V_{IN} \geq V_{SS}$	- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled	- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} and CE2 = V_{IH}, $I_{I/O}$ = 0mA, Others at V_{IL} or V_{IH}	-	30	55	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH} or CE2 = V_{IL} Others at V_{IL} or V_{IH}	-	0.3	5	mA
	I_{SB1}	CE# $\geq V_{CC}$-0.2V or CE2$\leq$0.2V Others at 0.2V or V_{CC}-0.2V	-	1	50	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (T_A = 25℃ , f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY65W64-25		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	25	-	ns
Address Access Time	t_{AA}	-	25	ns
Chip Enable Access Time	t_{ACE}	-	25	ns
Output Enable Access Time	t_{OE}	-	9	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	4	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	9	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	LY65W64-25		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	25	-	ns
Address Valid to End of Write	t_{AW}	20	-	ns
Chip Enable to End of Write	t_{CW}	20	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	12	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	10	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	6	-	ns
Write to Output in High-Z	t_{WHZ}*	-	10	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)
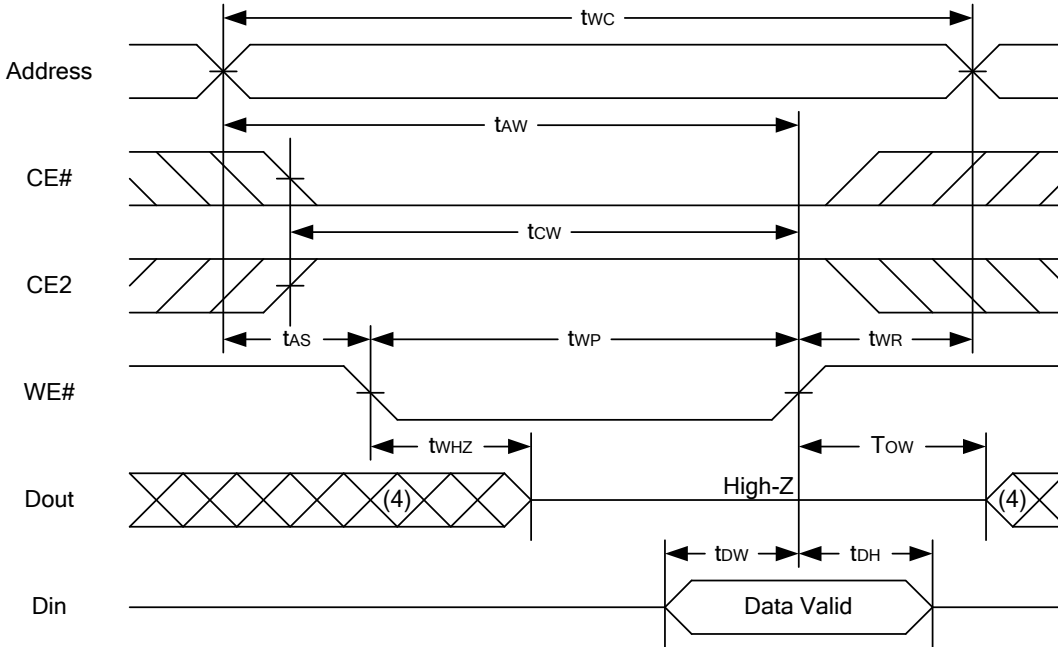
## WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)
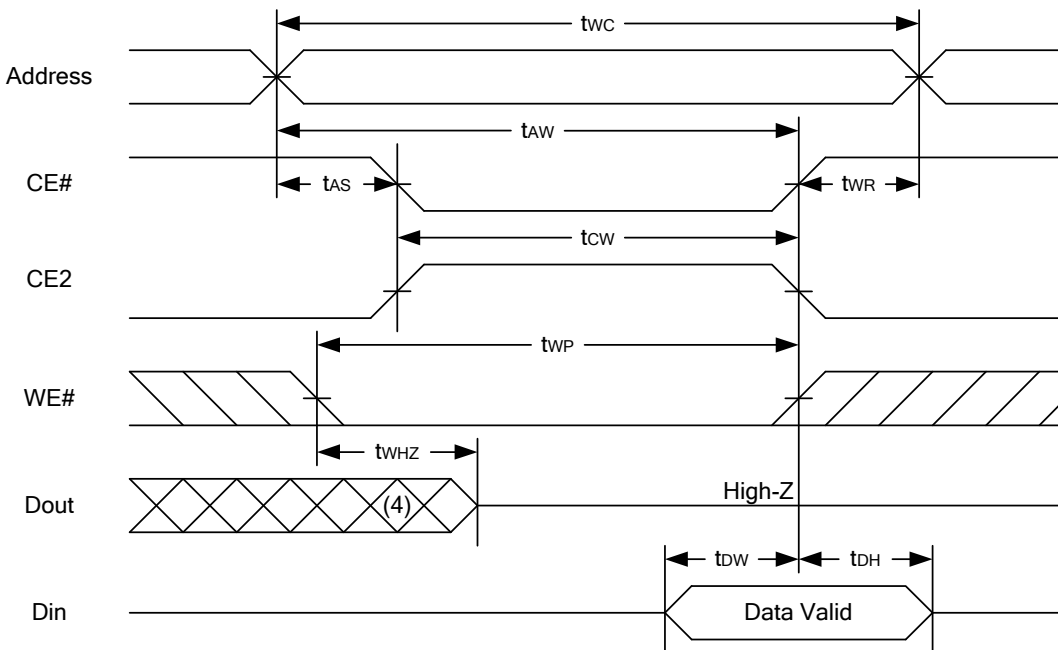
Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

| PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# $\geq$ V_{CC} - 0.2V or CE2 $\leq$ 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V CE# $\geq$ V_{CC} - 0.2V or CE2 $\leq$ 0.2V Others at 0.2V or V_{CC}-0.2V	-	0.5	30	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM
Low Vcc Data Retention Waveform (1) (CE# controlled)
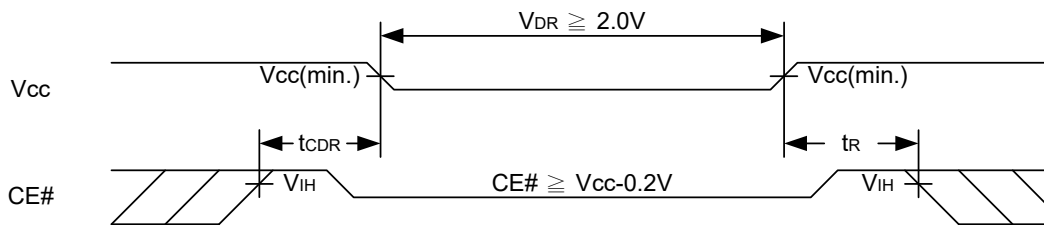
Low Vcc Data Retention Waveform (2) (CE2 controlled)
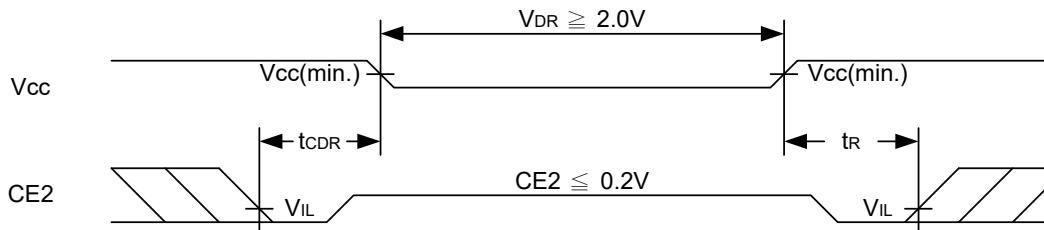
PACKAGE OUTLINE DIMENSION

28 pin 8x13.4mm sTSOP Package Outline Dimension
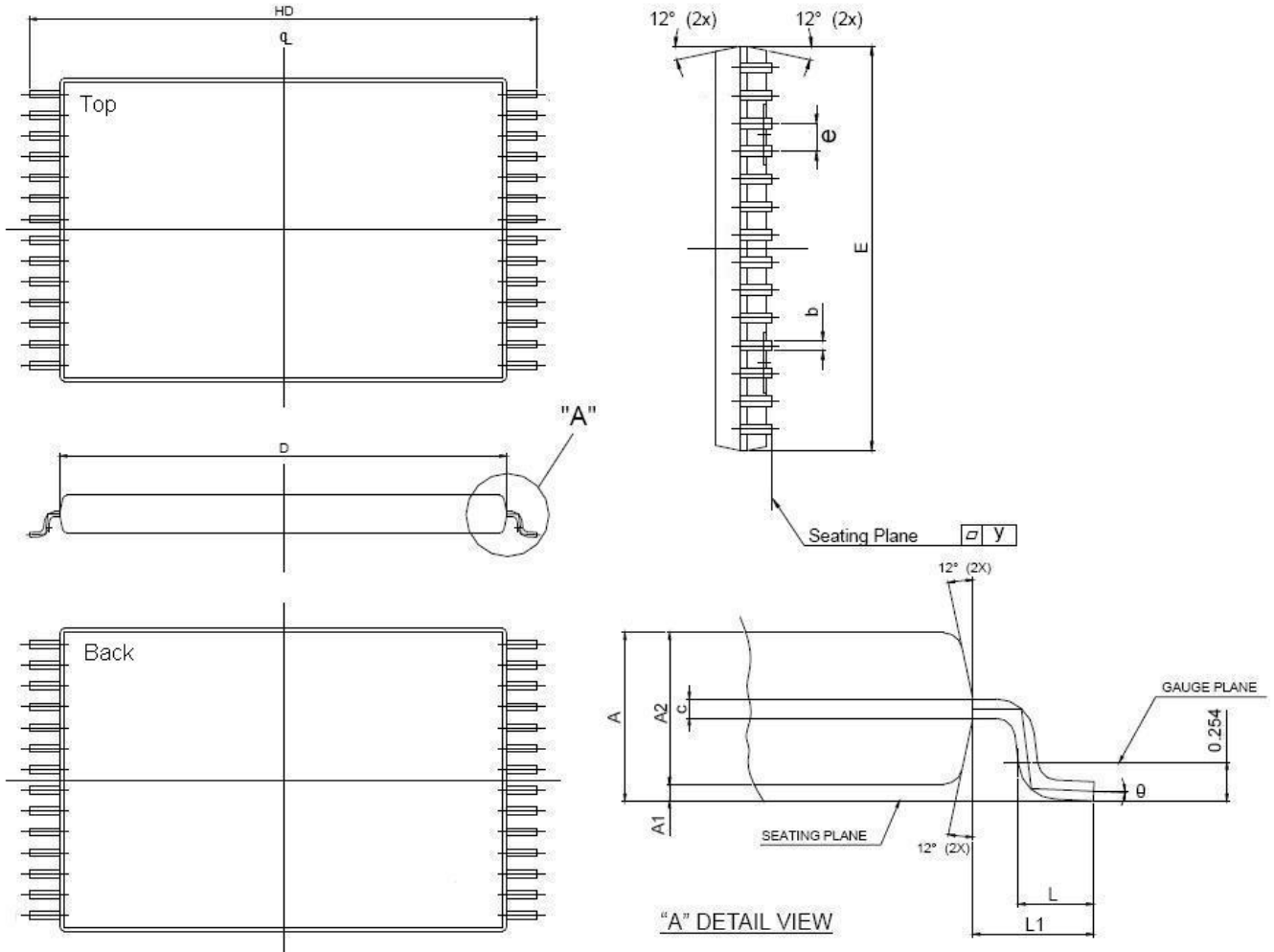
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
Θ	0°	3°	5°	0°	3°	5°

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32Pin (8mmx13.4mm) sTSOP	25	Ultra Low Power	0℃~70℃	Tray	LY65W64RL-25LL
				Tape Reel	LY65W64RL-25LLT
			-40℃~85℃	Tray	LY65W64RL-25LLI
				Tape Reel	LY65W64RL-25LLIT

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