REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Aug.29.2005
Rev. 1.1	Revised I_{SB1}/I_{DR}/Test Condition of I_{CC}	Oct.31.2005
Rev. 1.2	Adding PKG type : 32 P-DIP Revised Test Condition of I_{SB1}/I_{DR}	May.14.2007
Rev. 2.0	Adding SL Spec. Revised **ABSOLUTE MAXIMUN RATINGS**	Jul.26.2007
Rev. 2.1	Added I_{SB1}/I_{DR} values when T_A = 25℃ and T_A = 40℃ Revised $I_{SB1\ (MAX)}$ of SL grade Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Added packing type in **ORDERING INFORMATION** Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS** Revised -35ns to -45ns Spec.	Mar.30.2009
Rev. 2.2	Revised V_{DR}	Sep.11.2009
Rev. 2.3	Revised **PACKAGE OUTLINE DIMENSION** in page 8/9/11	May.7.2010
Rev. 2.4	Revised **ORDERING INFORMATION** in page 12	Aug.30.2010
Rev. 2.5	Revised $V_{IL(max)}$ from 0.6V to 0.8V	May 8.2014
Rev. 2.6	Correct **ORDERING INFORMATION** Typo.	May.20.2016
Rev. 2.7	Deleted **WRITE CYCLE** Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions in page 6. Revised **ORDERING INFORMATION** in page 14	Jun.28.2016
Rev. 2.8	Removed Package Type : PDIP	Apr.08. 2019
Rev. 2.9	Revised ORDERING INFORMATION in page 11 32 Pin(450mil) SOP PackingType : Tube→Tray	Aug.24.2023

Lyontek Inc.

LY622568

Rev. 2.9

256K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Fast access time : 45/55/70ns
- Low power consumption:
  Operating current : 50/40/30mA (TYP.)
  Standby current : 3μA@5V(TYP.) LL/SL version
  2μA@3V(TYP.) SL version
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450 mil SOP
  32-pin 8mm x 20mm TSOP I
  32-pin 8mm x 13.4mm sTSOP

GENERAL DESCRIPTION

The LY622568 is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

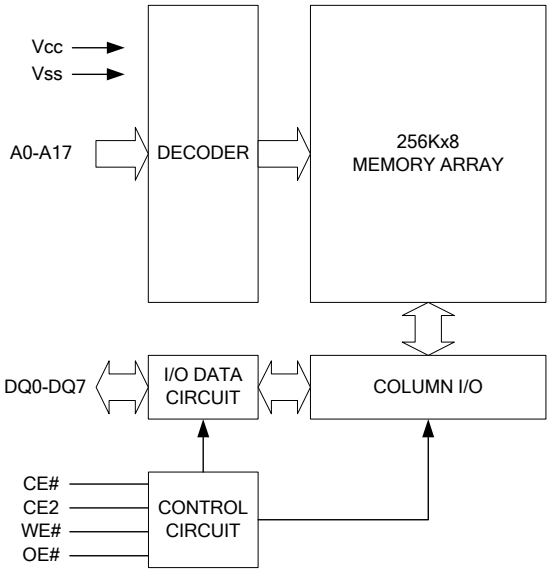
The LY622568 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY622568 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		
				Standby(ISB1,TYP.)		Operating(Icc,TYP.)
LY622568(LL)	0 ~ 70℃	4.5 ~ 5.5V	45/55/70ns	-	3μA@5V	50/40/30mA
LY622568(LLE)	-20 ~ 80℃	4.5 ~ 5.5V	45/55/70ns	-	3μA@5V	50/40/30mA
LY622568(LLI)	-40 ~ 85℃	4.5 ~ 5.5V	45/55/70ns	-	3μA@5V	50/40/30mA
LY622568(SL)	0 ~ 70℃	4.5 ~ 5.5V	45/55/70ns	2μA@3V	3μA@5V	50/40/30mA
LY622568(SLE)	-20 ~ 80℃	4.5 ~ 5.5V	45/55/70ns	2μA@3V	3μA@5V	50/40/30mA
LY622568(SLI)	-40 ~ 85℃	4.5 ~ 5.5V	45/55/70ns	2μA@3V	3μA@5V	50/40/30mA

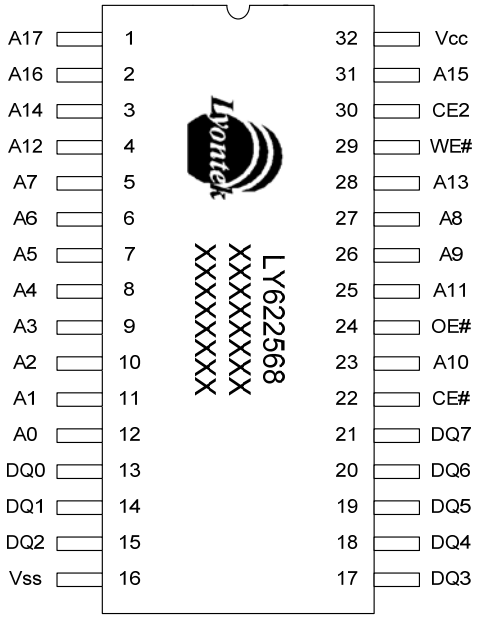
FUNCTIONAL BLOCK DIAGRAM



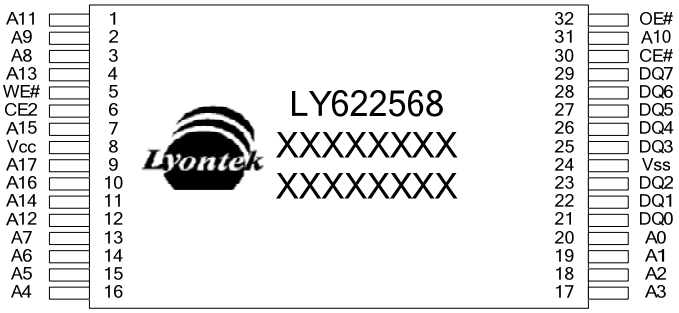
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION



SOP



TSOP I /sTSOP

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB1}
	X	L	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC},I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Input High Voltage	V_{IH}*1			2.4	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}*2			- 0.2	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} and CE2 = V_{IH} , $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	- 45	-	50	80	mA
			- 55	-	40	60	mA
			- 70	-	30	50	mA
	I_{CC1}	Cycle time = 1µs CE# = 0.2V and CE2$\geqq$$V_{CC}$-0.2V, $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC} - 0.2V		-	4	10	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq$$V_{CC}$-0.2V or CE2$\leqq$0.2V Others at 0.2V or V_{CC} - 0.2V	LL/LLE/LLI	-	3	50	µA
			SL*5 SLE*5 SLI*5 25℃	-	2	5	µA
			SL*5 SLE*5 SLI*5 40℃	-	2	5	µA
			SL	-	3	20	µA
			SLE/SLI	-	3	25	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -2mA/4mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY622568-45		LY622568-55		LY622568-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	45	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	15	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

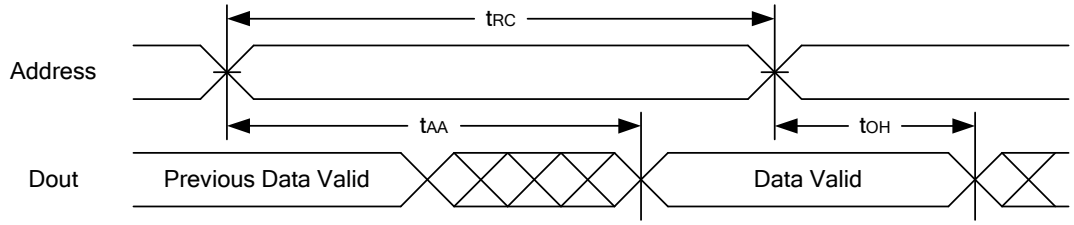
(2) WRITE CYCLE

PARAMETER	SYM.	LY622568-45		LY622568-55		LY622568-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	40	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	40	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

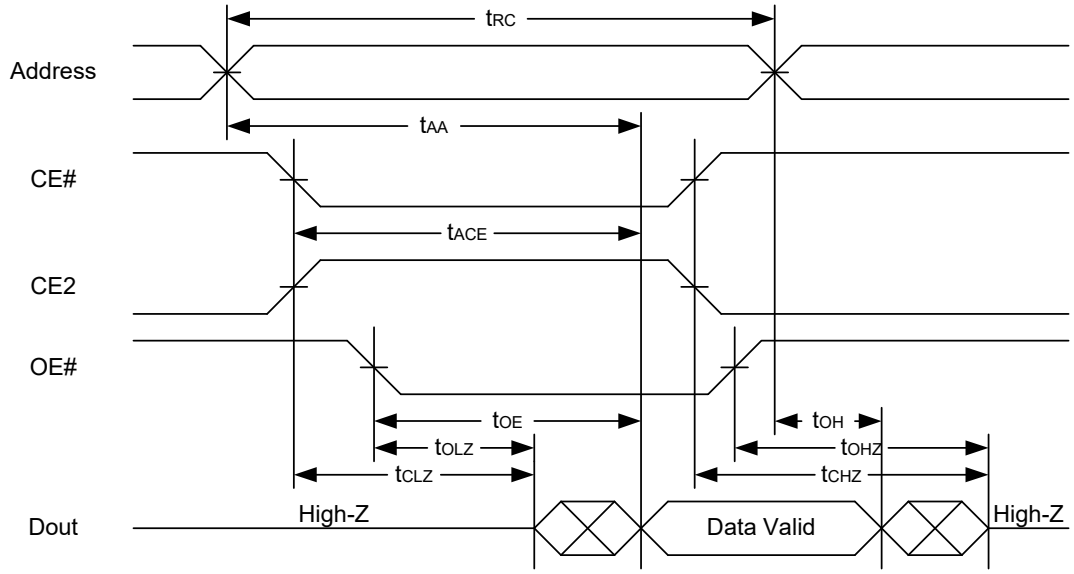
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

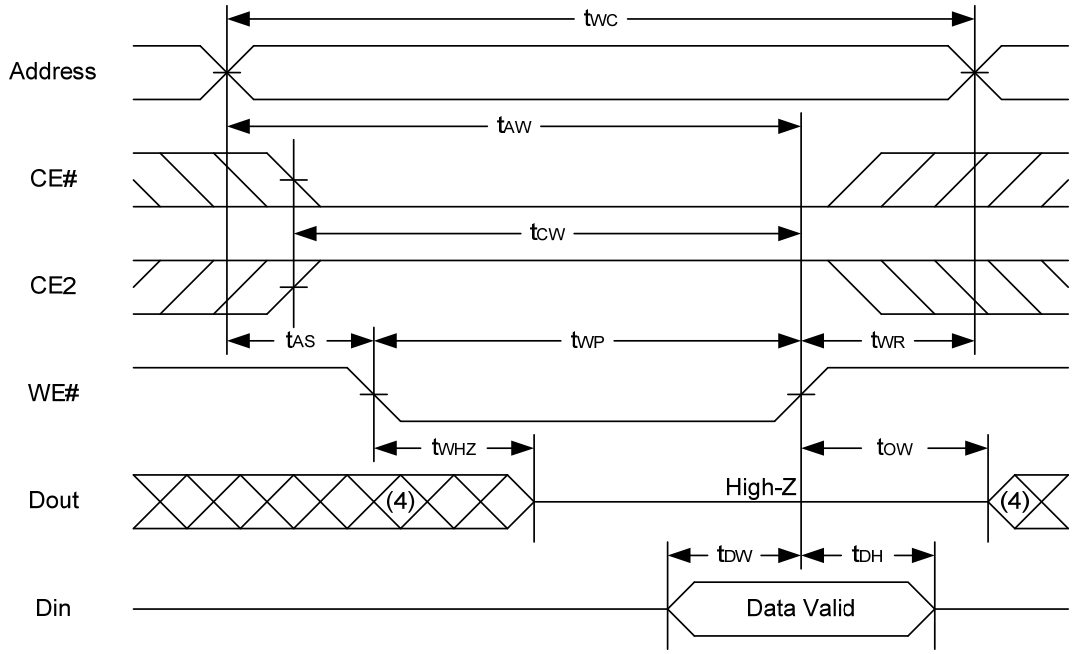


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

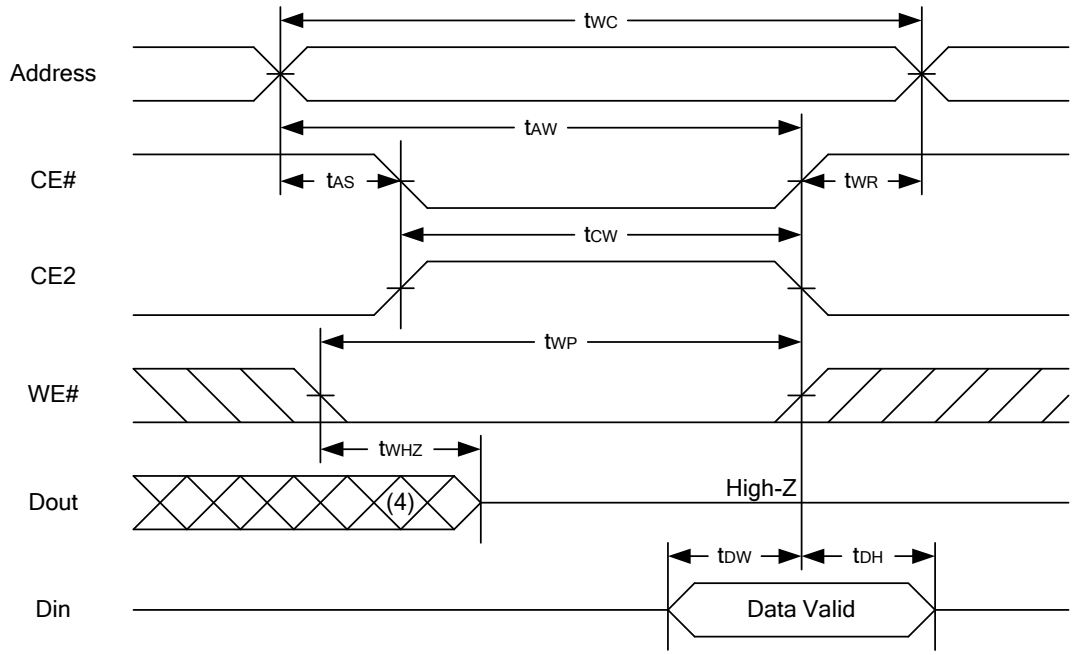


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low., CE2 = high.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :
1.A write occurs during the overlap of a low CE#, high CE2, low WE#.
2.During a WE#controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3.During this period, I/O pins are in the output state, and input signals must not be applied.
4.If the CE#low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

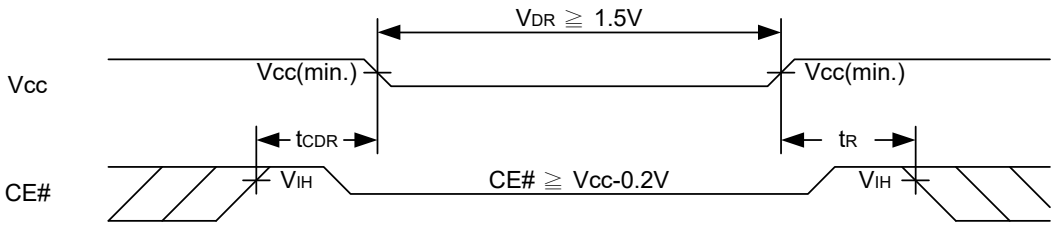
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V			1.5	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V Other pins at 0.2V or V_{CC}-0.2V	LL		-	1	20	µA
			SL	25℃	-	1	4	µA
				40℃	-	1	4	µA
			SL		-	1	15	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC}*	-	-	ns

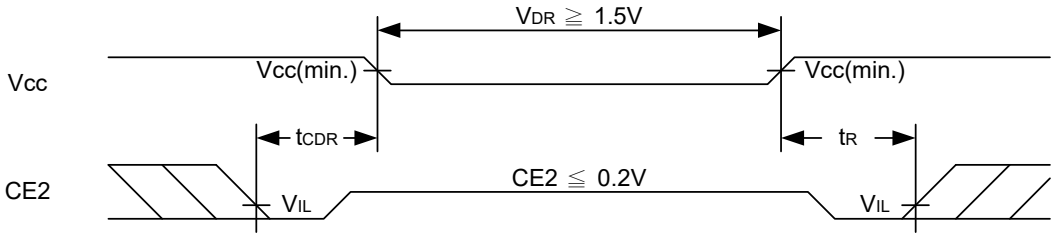
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)

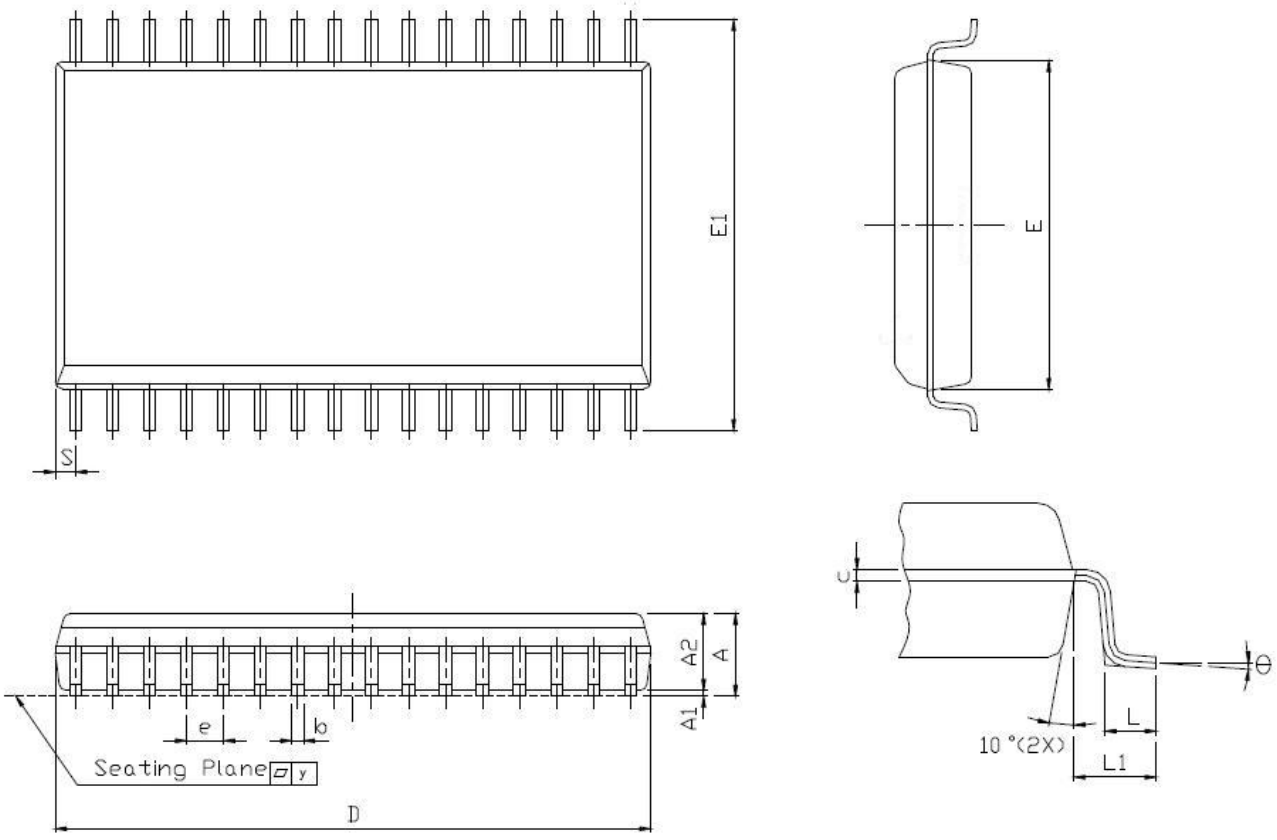


Low Vcc Data Retention Waveform (2) (CE2 controlled)



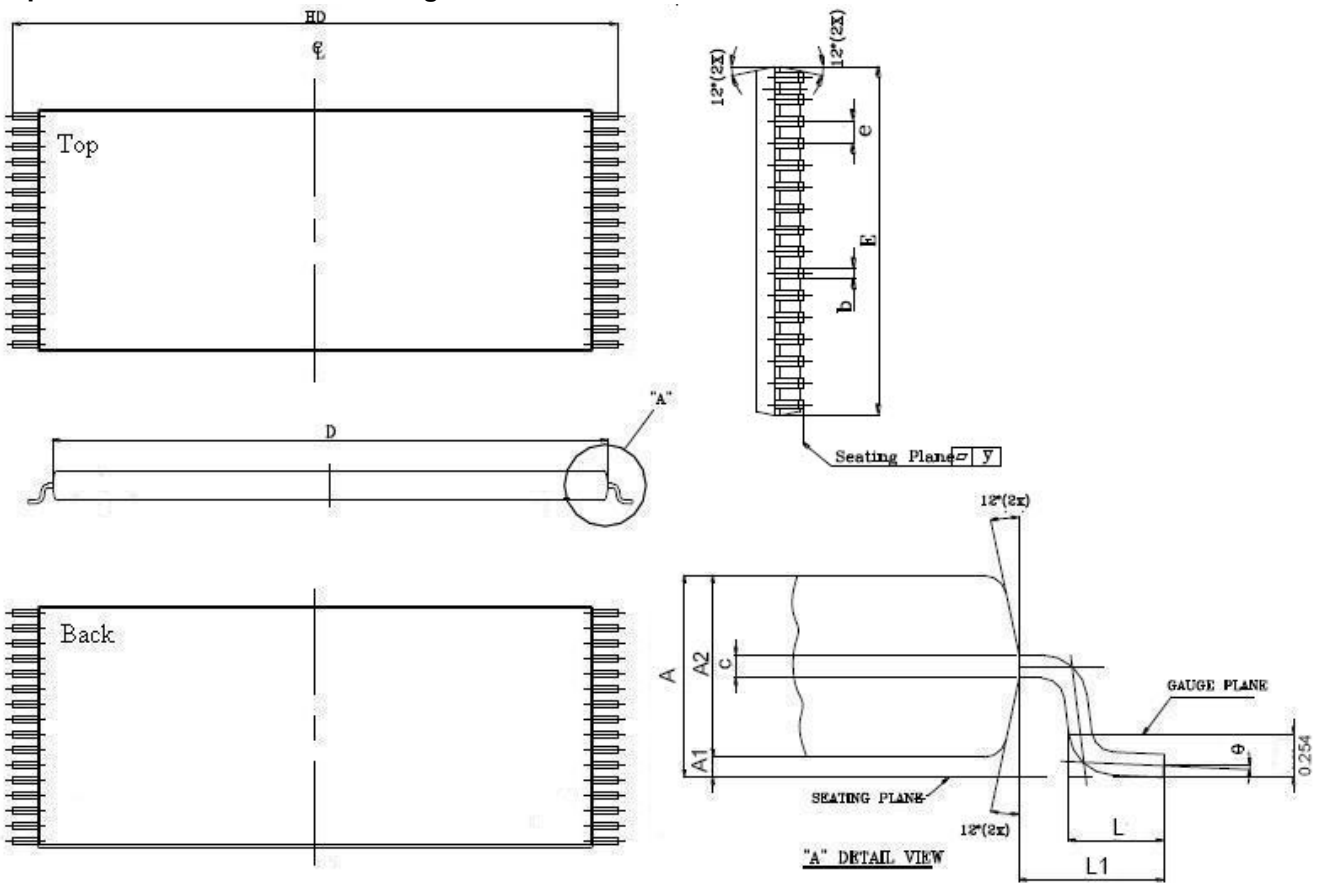
PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension



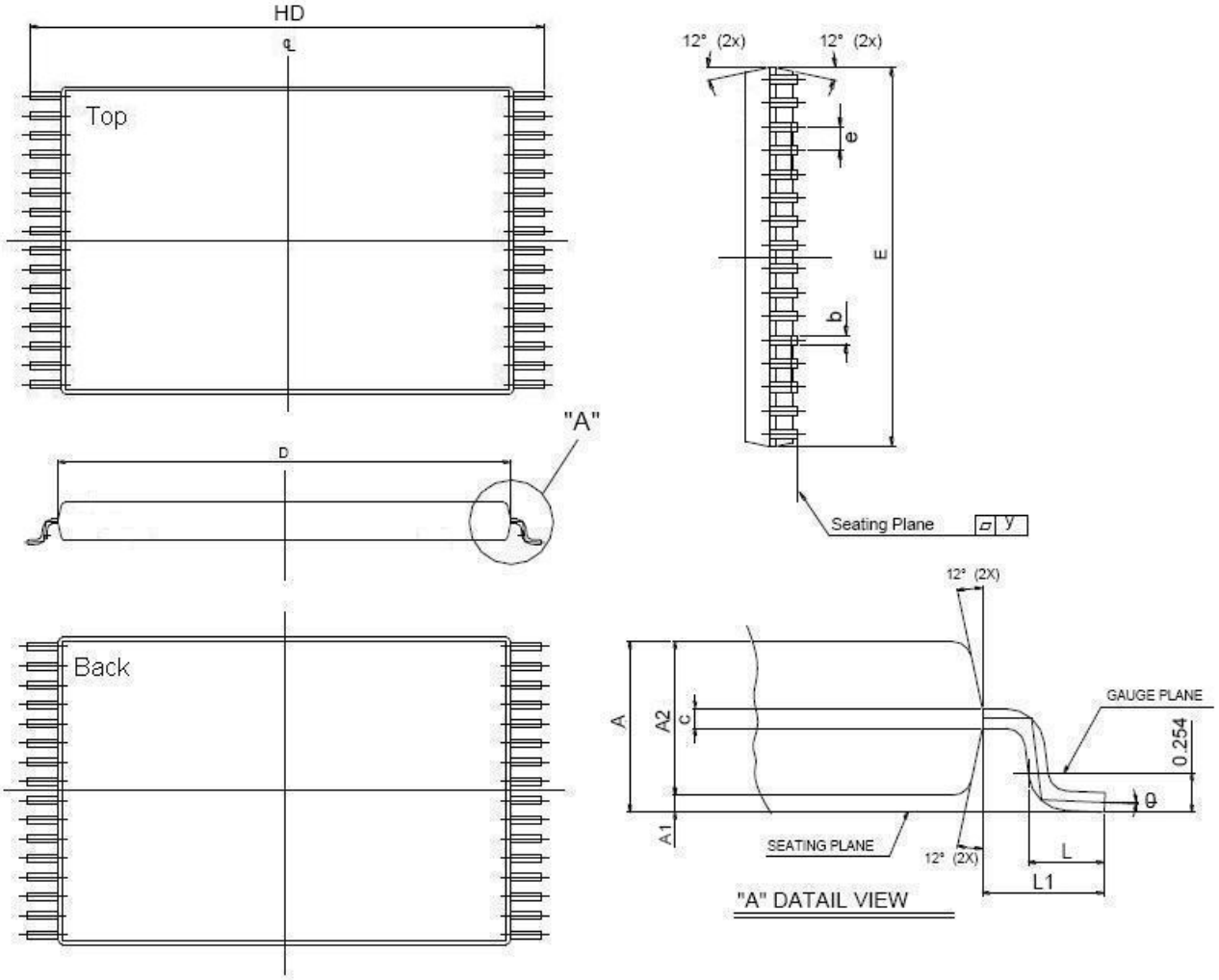
UNIT / SYM.	INCH.(BASE)	MM(REF)
A	0.120(MAX)	3.048(MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.116(MAX)	2.946(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445±0.006	11.303±0.152
E1	0.555±0.025	14.097±0.635
e	0.050(TYP)	1.270(TYP)
L	0.033±0.017	0.838±0.432
L1	0.055±0.008	1.397±0.203
S	0.026(MAX)	0.660(MAX)
y	0.004(MAX)	0.101(MAX)
Θ	0° -10°	0° -10°

32 pin 8mm x 20mm TSOP I Package Outline Dimension



UNIT / SYM.	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.724 ±0.008	18.40 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.024 ±0.004	0.60 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.08 (MAX)
Θ	0°~5°	0°~5°

32 pin 8mm x 13.4mm sTSOP Package Outline Dimension



SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.465 ±0.008	11.80 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.02 ±0.008	0.50 ±0.20
L1	0.031 ±0.005	0.8 ±0.125
y	0.003 (MAX)	0.076 (MAX)
Θ	0°~5°	0°~5°

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32Pin(450mil) SOP	45	Special Ultra Low Power	0℃~70℃	Tray	LY622568SL-45SL
				Tape Reel	LY622568SL-45SLT
			-20℃~80℃	Tray	LY622568SL-45SLE
				Tape Reel	LY622568SL-45SLET
			-40℃~85℃	Tray	LY622568SL-45SLI
				Tape Reel	LY622568SL-45SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568SL-45LL
				Tape Reel	LY622568SL-45LLT
			-20℃~80℃	Tray	LY622568SL-45LLE
				Tape Reel	LY622568SL-45LLET
			-40℃~85℃	Tray	LY622568SL-45LLI
				Tape Reel	LY622568SL-45LLIT
	55	Special Ultra Low Power	0℃~70℃	Tray	LY622568SL-55SL
				Tape Reel	LY622568SL-55SLT
			-20℃~80℃	Tray	LY622568SL-55SLE
				Tape Reel	LY622568SL-55SLET
			-40℃~85℃	Tray	LY622568SL-55SLI
				Tape Reel	LY622568SL-55SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568SL-55LL
				Tape Reel	LY622568SL-55LLT
			-20℃~80℃	Tray	LY622568SL-55LLE
				Tape Reel	LY622568SL-55LLET
			-40℃~85℃	Tray	LY622568SL-55LLI
				Tape Reel	LY622568SL-55LLIT
	70	Special Ultra Low Power	0℃~70℃	Tray	LY622568SL-70SL
				Tape Reel	LY622568SL-70SLT
			-20℃~80℃	Tray	LY622568SL-70SLE
				Tape Reel	LY622568SL-70SLET
			-40℃~85℃	Tray	LY622568SL-70SLI
				Tape Reel	LY622568SL-70SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568SL-70LL
				Tape Reel	LY622568SL-70LLT
			-20℃~80℃	Tray	LY622568SL-70LLE
				Tape Reel	LY622568SL-70LLET
			-40℃~85℃	Tray	LY622568SL-70LLI
				Tape Reel	LY622568SL-70LLIT

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32Pin (8mmx20mm) TSOP I	45	Special Ultra Low Power	0℃~70℃	Tray	LY622568LL-45SL
				Tape Reel	LY622568LL-45SLT
			-20℃~80℃	Tray	LY622568LL-45SLE
				Tape Reel	LY622568LL-45SLET
			-40℃~85℃	Tray	LY622568LL-45SLI
				Tape Reel	LY622568LL-45SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568LL-45LL
				Tape Reel	LY622568LL-45LLT
			-20℃~80℃	Tray	LY622568LL-45LLE
				Tape Reel	LY622568LL-45LLET
			-40℃~85℃	Tray	LY622568LL-45LLI
				Tape Reel	LY622568LL-45LLIT
	55	Special Ultra Low Power	0℃~70℃	Tray	LY622568LL-55SL
				Tape Reel	LY622568LL-55SLT
			-20℃~80℃	Tray	LY622568LL-55SLE
				Tape Reel	LY622568LL-55SLET
			-40℃~85℃	Tray	LY622568LL-55SLI
				Tape Reel	LY622568LL-55SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568LL-55LL
				Tape Reel	LY622568LL-55LLT
			-20℃~80℃	Tray	LY622568LL-55LLE
				Tape Reel	LY622568LL-55LLET
			-40℃~85℃	Tray	LY622568LL-55LLI
				Tape Reel	LY622568LL-55LLIT
	70	Special Ultra Low Power	0℃~70℃	Tray	LY622568LL-70SL
				Tape Reel	LY622568LL-70SLT
			-20℃~80℃	Tray	LY622568LL-70SLE
				Tape Reel	LY622568LL-70SLET
			-40℃~85℃	Tray	LY622568LL-70SLI
				Tape Reel	LY622568LL-70SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568LL-70LL
				Tape Reel	LY622568LL-70LLT
			-20℃~80℃	Tray	LY622568LL-70LLE
				Tape Reel	LY622568LL-70LLET
			-40℃~85℃	Tray	LY622568LL-70LLI
				Tape Reel	LY622568LL-70LLIT

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32Pin (8mmx13.4mm) sTSOP	45	Special Ultra Low Power	0℃~70℃	Tray	LY622568RL-45SL
				Tape Reel	LY622568RL-45SLT
			-20℃~80℃	Tray	LY622568RL-45SLE
				Tape Reel	LY622568RL-45SLET
			-40℃~85℃	Tray	LY622568RL-45SLI
				Tape Reel	LY622568RL-45SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568RL-45LL
				Tape Reel	LY622568RL-45LLT
			-20℃~80℃	Tray	LY622568RL-45LLE
				Tape Reel	LY622568RL-45LLET
			-40℃~85℃	Tray	LY622568RL-45LLI
				Tape Reel	LY622568RL-45LLIT
	55	Special Ultra Low Power	0℃~70℃	Tray	LY622568RL-55SL
				Tape Reel	LY622568RL-55SLT
			-20℃~80℃	Tray	LY622568RL-55SLE
				Tape Reel	LY622568RL-55SLET
			-40℃~85℃	Tray	LY622568RL-55SLI
				Tape Reel	LY622568RL-55SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568RL-55LL
				Tape Reel	LY622568RL-55LLT
			-20℃~80℃	Tray	LY622568RL-55LLE
				Tape Reel	LY622568RL-55LLET
			-40℃~85℃	Tray	LY622568RL-55LLI
				Tape Reel	LY622568RL-55LLIT
	70	Special Ultra Low Power	0℃~70℃	Tray	LY622568RL-70SL
				Tape Reel	LY622568RL-70SLT
			-20℃~80℃	Tray	LY622568RL-70SLE
				Tape Reel	LY622568RL-70SLET
			-40℃~85℃	Tray	LY622568RL-70SLI
				Tape Reel	LY622568RL-70SLIT
		Ultra Low Power	0℃~70℃	Tray	LY622568RL-70LL
				Tape Reel	LY622568RL-70LLT
			-20℃~80℃	Tray	LY622568RL-70LLE
				Tape Reel	LY622568RL-70LLET
			-40℃~85℃	Tray	LY622568RL-70LLI
				Tape Reel	LY622568RL-70LLIT

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