



### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Sep.23.2020
Rev. 1.1	Revised DC ELECTRICAL CHARACTERISTICS of Standby Power Supply Current / ISB1 SL MAX.=5 , SLI MAX.=10 in page 4	June.10.2022
Rev. 1.2	Revised ORDERING INFORMATION in page 14 32 Pin(450mil) SOP PackingType : Tube→Tray	Aug.24.2023

### FEATURES

- Fast access time : 45/55ns
- Low power consumption:  
Operating current : 12/10mA (TYP.)  
Standby current : 1 $\mu$ A (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450mil SOP  
32-pin 600mil PDIP  
32-pin 8mm x 20mm TSOP I  
32-pin 8mm x 13.4mm sTSOP  
36-ball 6mm x 8mm TFBGA

### GENERAL DESCRIPTION

The LY62L2568B is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

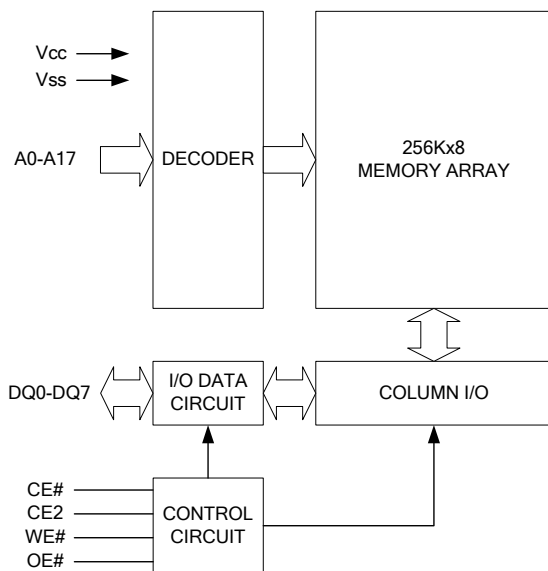
The LY62L2568B is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L2568B operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible.

### PRODUCT FAMILY

Product Family	Operating Temperature	V <sub>CC</sub> Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> , TYP.)	Operating(I <sub>CC</sub> , TYP.)
LY62L2568B	0 ~ 70°C	2.7 ~ 3.6V	45/55ns	1 $\mu$ A	12/10mA
LY62L2568B(I)	-40 ~ 85°C	2.7 ~ 3.6V	45/55ns	1 $\mu$ A	12/10mA

### FUNCTIONAL BLOCK DIAGRAM

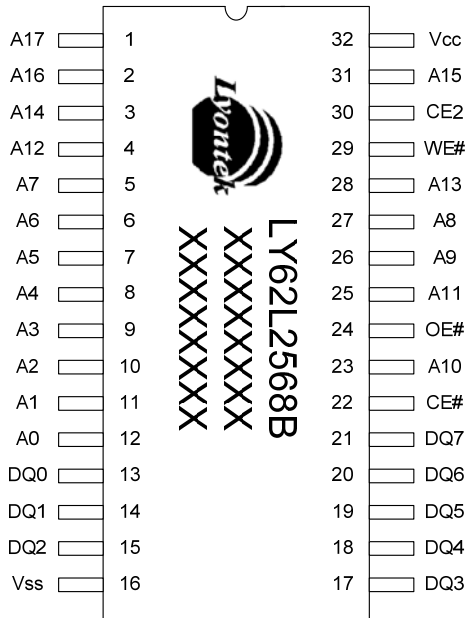


### PIN DESCRIPTION

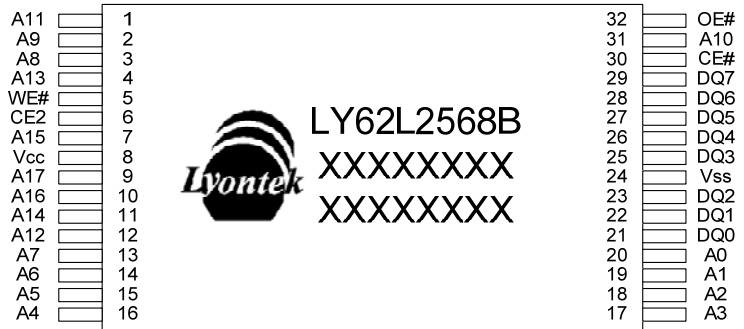
SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground
NC	No Connection



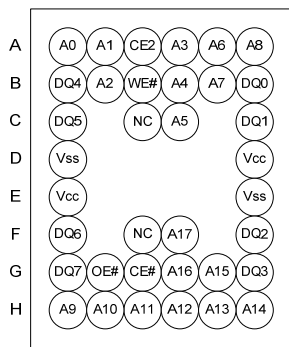
### PIN CONFIGURATION



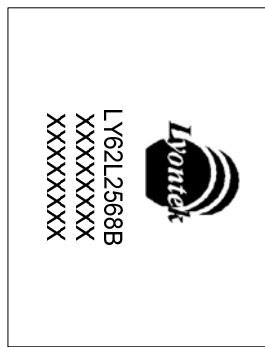
SOP / PDIP



TSOP I / sTSOP



TFPGA (See through with Top View)



TFPGA (Top View)



#### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to V <sub>SS</sub>	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

#### TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I <sub>SB1</sub>
	X	L	X	X	High-Z	I <sub>SB1</sub>
Output Disable	L	H	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*4	MAX.	UNIT		
Supply Voltage	V <sub>CC</sub>		2.7	3.0	3.6	V		
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>		2.2	-	V <sub>CC</sub> +0.3	V		
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>		-0.2	-	0.6	V		
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA		
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.2	2.7	-	V		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = MIN. CE# = 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-45	-	12	20	mA	
			-55	-	10	17	mA	
	I <sub>CC1</sub>	Cycle time = 1μs CE# = 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-	3	5	mA		
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	SL <sup>*5</sup>	25°C	-	1	3	μA
			SLI <sup>*5</sup>	40°C	-	1	3	μA
			SL		-	1	5	μA
			SLI		-	1	10	μA

**Notes:**

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V

**CAPACITANCE ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	$C_{IN}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to $V_{CC} - 0.2\text{V}$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$ , $I_{OH}/I_{OL} = -1\text{mA}/2\text{mA}$

**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

PARAMETER	SYM.	LY62L2568B-45		LY62L2568B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	$t_{RC}$	45	-	55	-	ns
Address Access Time	$t_{AA}$	-	45	-	55	ns
Chip Enable Access Time	$t_{ACE}$	-	45	-	55	ns
Output Enable Access Time	$t_{OE}$	-	20	-	25	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	15	-	20	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	15	-	20	ns
Output Hold from Address Change	$t_{OH}$	10	-	10	-	ns

**(2) WRITE CYCLE**

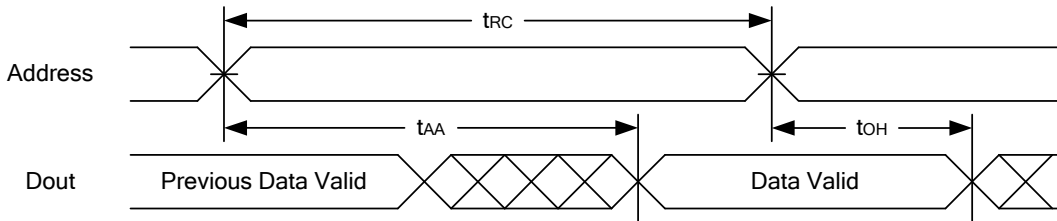
PARAMETER	SYM.	LY62L2568B-45		LY62L2568B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	$t_{WC}$	45	-	55	-	ns
Address Valid to End of Write	$t_{AW}$	40	-	50	-	ns
Chip Enable to End of Write	$t_{CW}$	40	-	50	-	ns
Address Set-up Time	$t_{AS}$	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	35	-	45	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	ns
Data to Write Time Overlap	$t_{DW}$	20	-	25	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	15	-	20	ns

\*These parameters are guaranteed by device characterization, but not production tested.

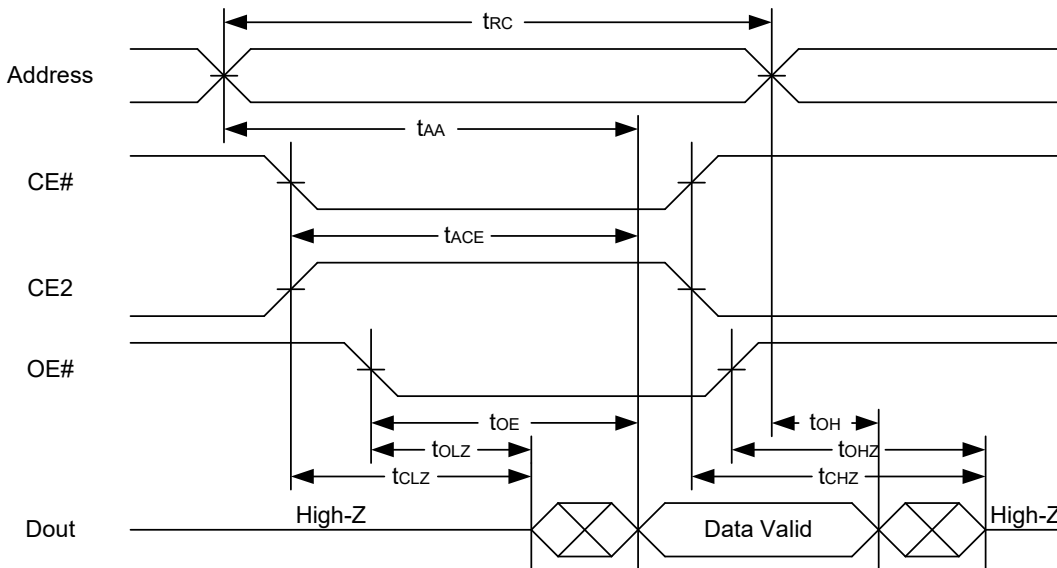


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



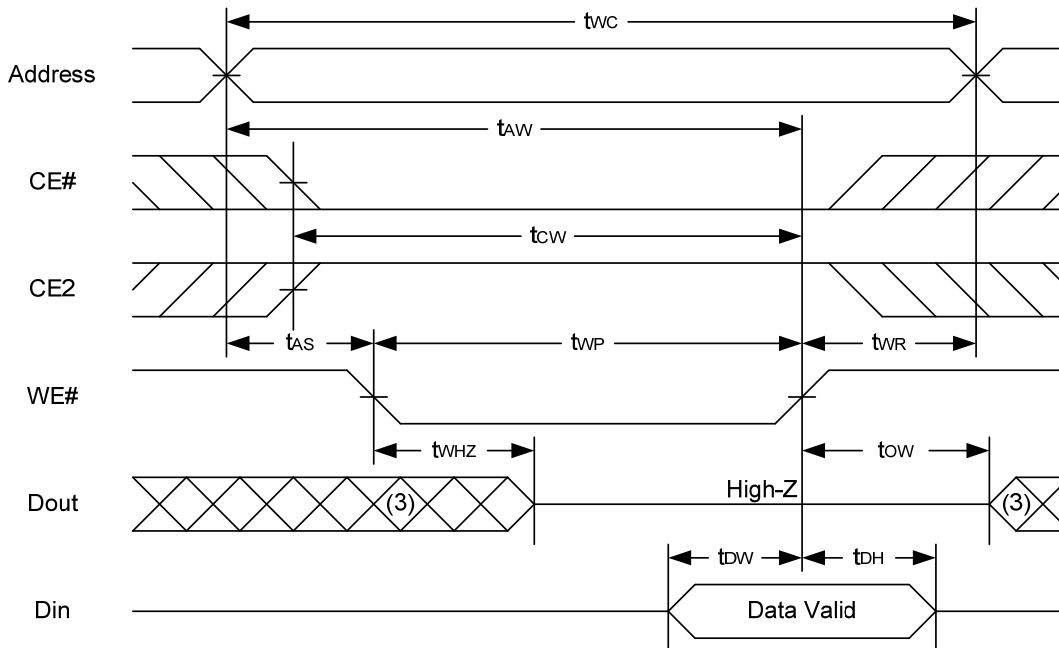
#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



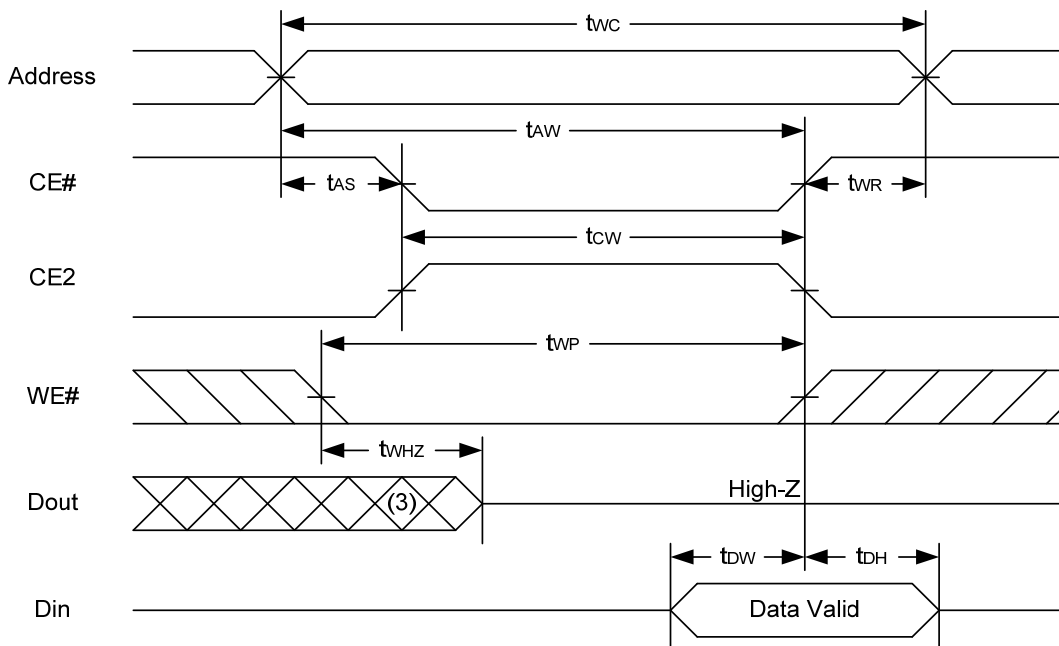
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



### WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.





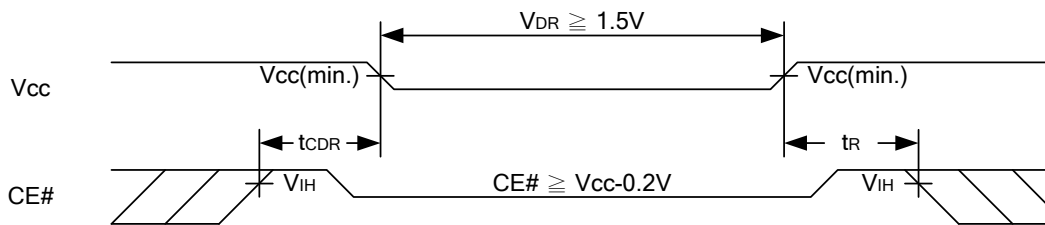
**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	1.5	-	3.6	V		
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	SL	25°C	-	1	3	μA
			SLI	40°C	-	1	3	μA
			SL		-	1	5	μA
			SLI		-	1	10	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns		

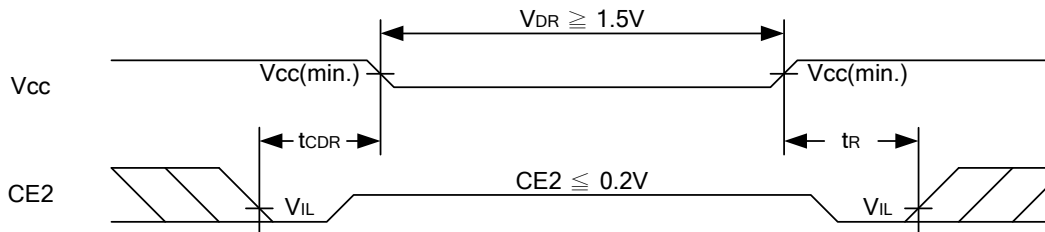
t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**

**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**



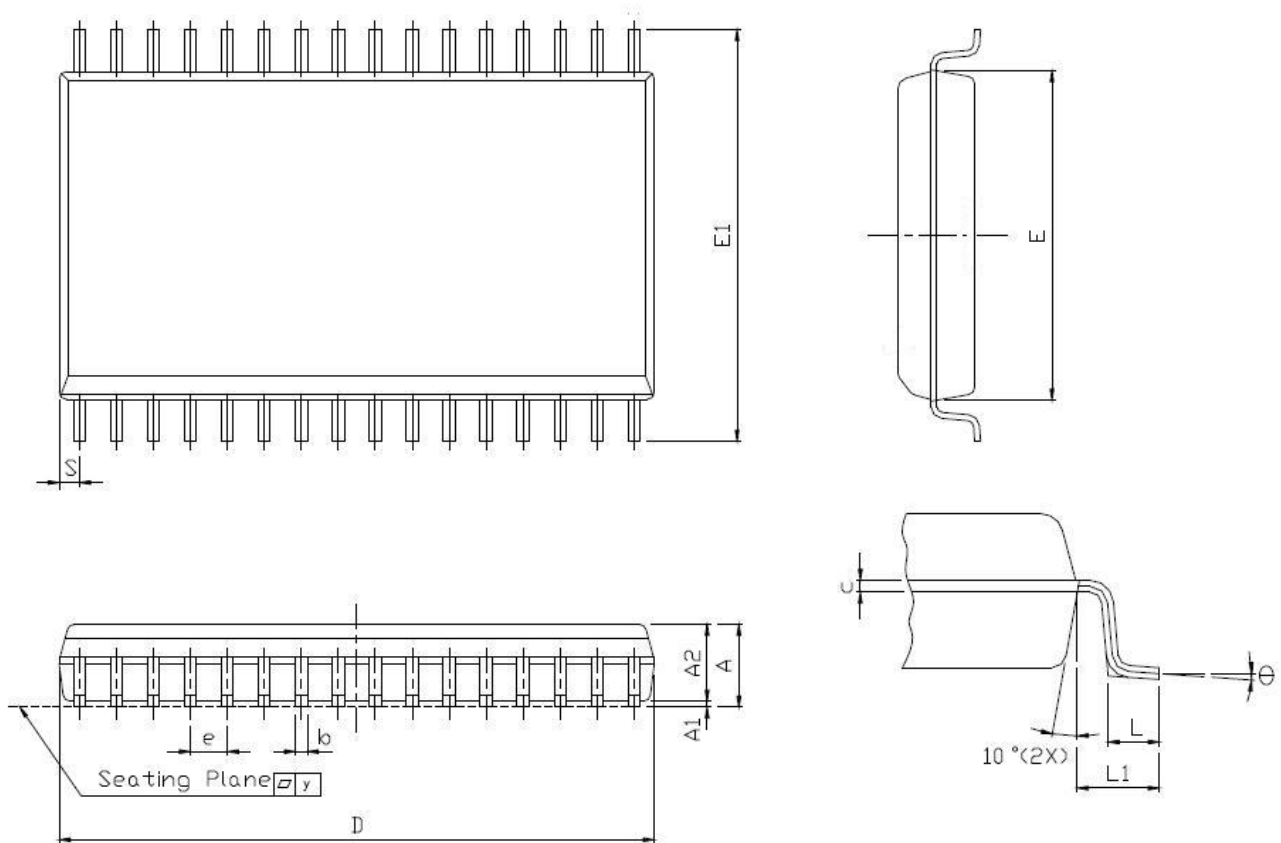
**Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)**





### PACKAGE OUTLINE DIMENSION

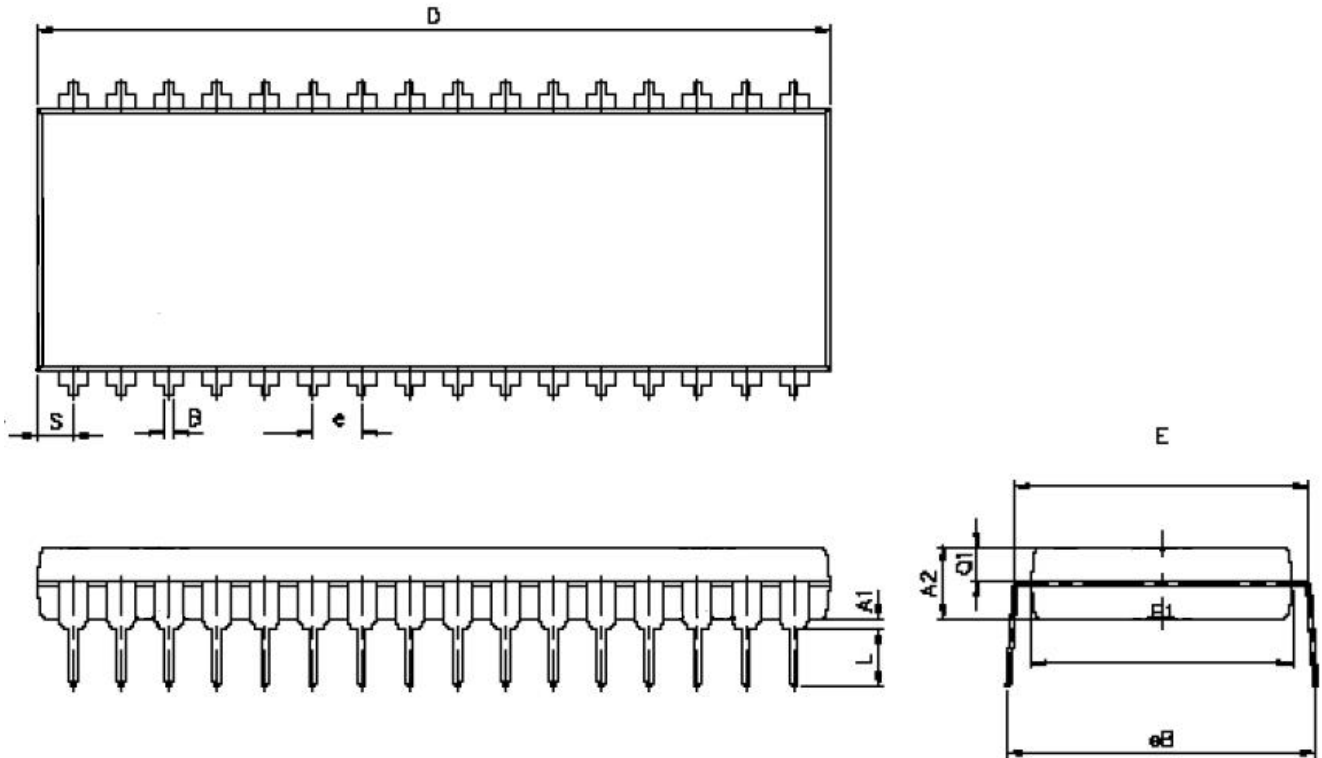
#### 32-pin 450 mil SOP Package Outline Dimension



SYM.	UNIT	INCH.(BASE)	MM(REF)
A		0.120(MAX)	3.048(MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.116(MAX)	2.946(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445±0.006	11.303±0.152
E1		0.555±0.025	14.097±0.635
e		0.050(TYP)	1.270(TYP)
L		0.033±0.017	0.838±0.432
L1		0.055±0.008	1.397±0.203
S		0.026(MAX)	0.660(MAX)
y		0.004(MAX)	0.101(MAX)
Θ		0° -10°	0° -10°



#### 32-pin 600 mil PDIP Package Outline Dimension

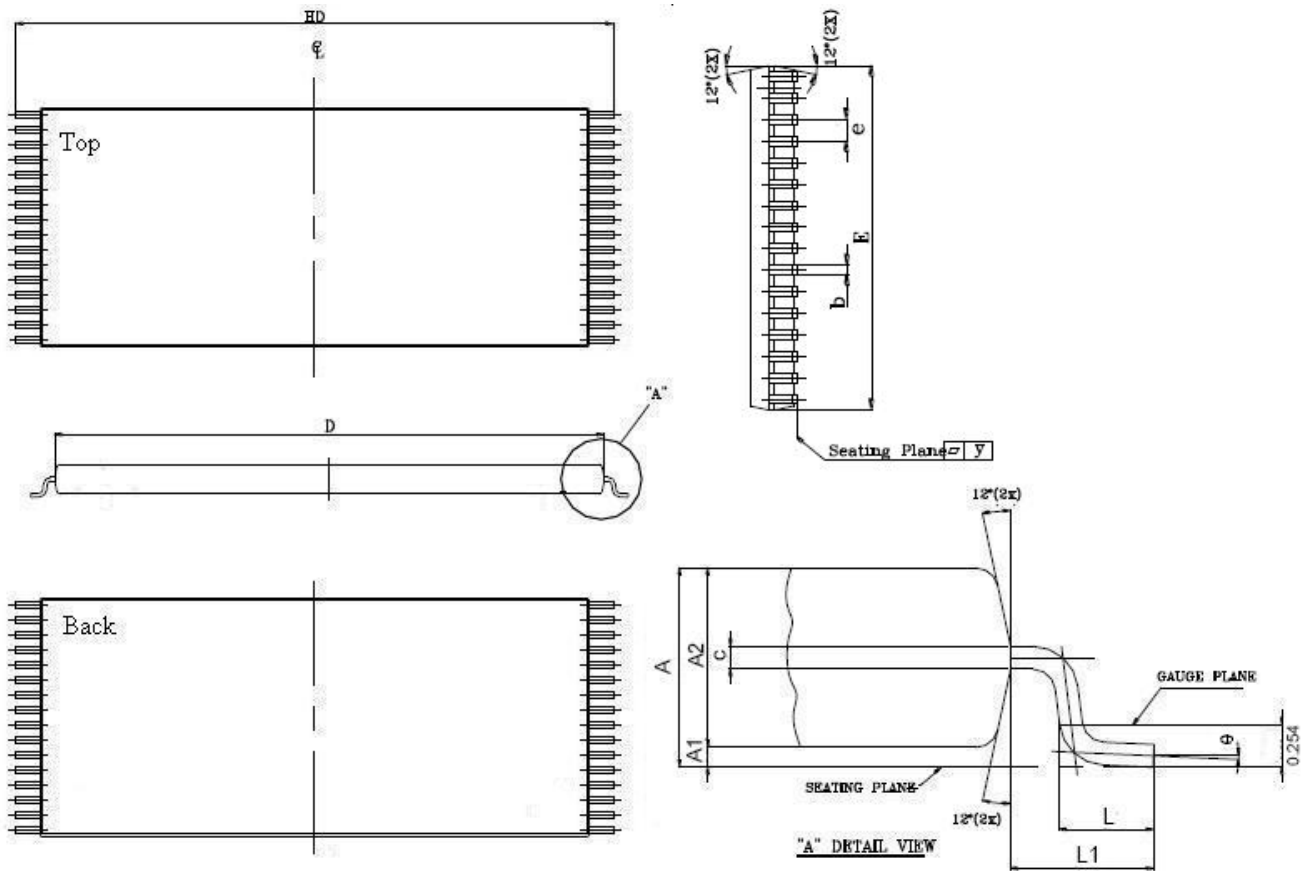


SYM. \ UNIT	INCH(BASE)	MM(REF)
A1	0.015(MIN)	0.381(MIN)
A2	0.155±0.005	3.937±0.127
B	0.018±0.005	0.457±0.127
D	1.650±0.01	41.910±0.254
E	0.600±0.010	15.240±0.254
E1	0.545±0.005	13.843±0.127
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508.
L	0.158±0.043	4.013±1.092
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127

Note : D/E1/S dimension do not include mold flash.

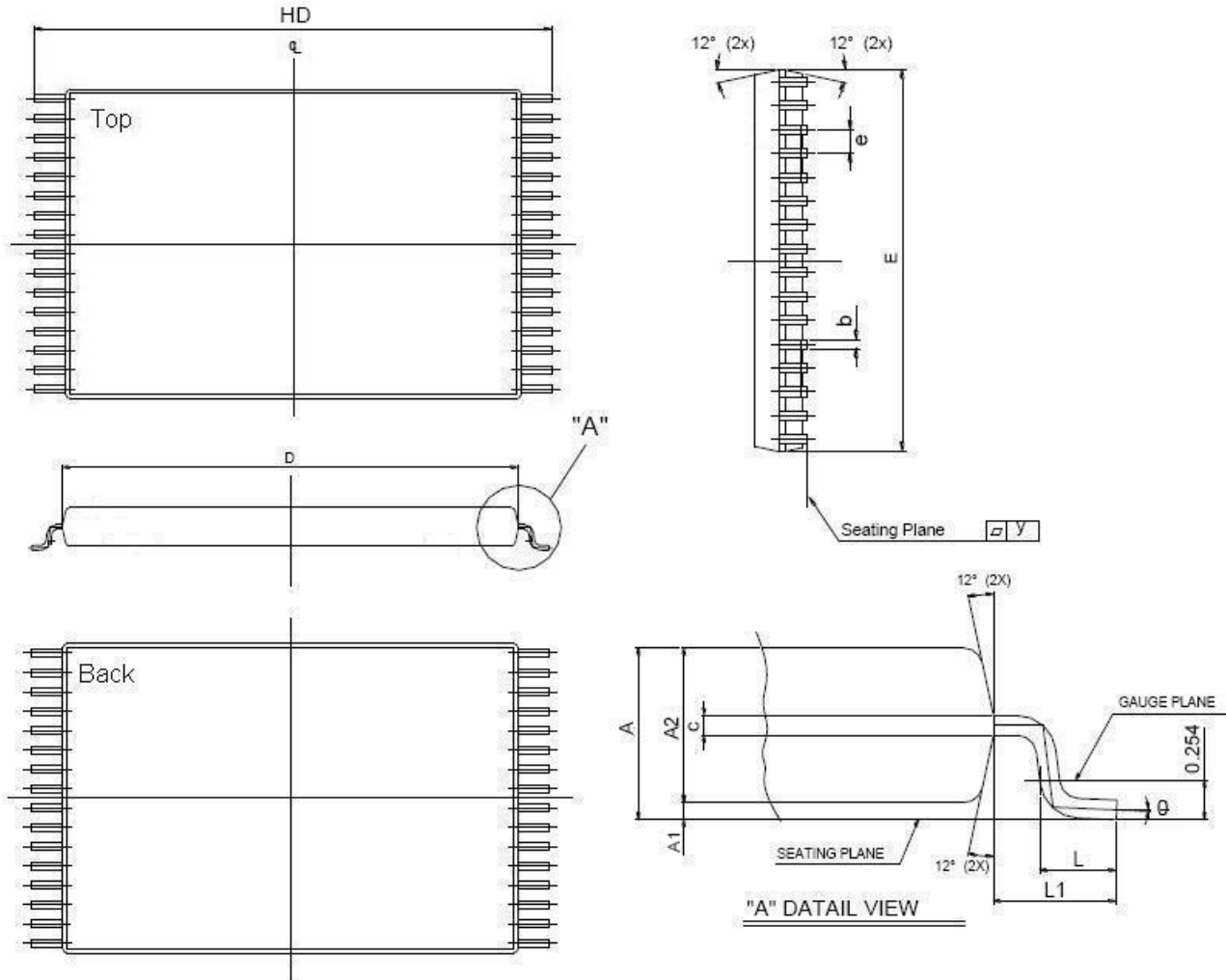


**32-pin 8mm x 20mm TSOP I Package Outline Dimension**



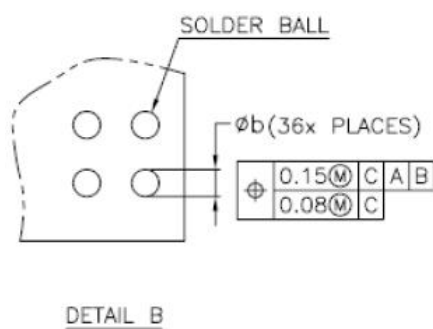
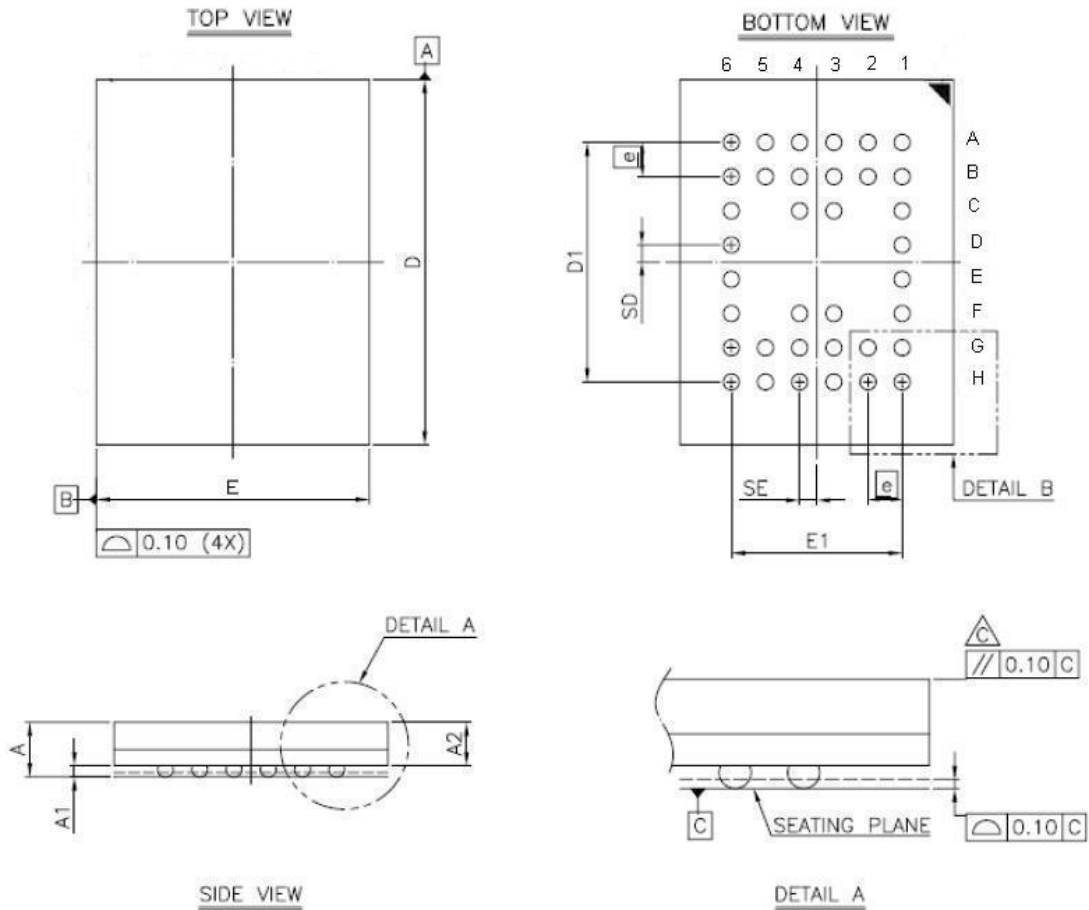
SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.724 ±0.008	18.40 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.024 ±0.004	0.60 ±0.10
L1		0.0315 ±0.004	0.08 ±0.10
y		0.003 (MAX)	0.08 (MAX)
∅		0°~5°	0°~5°

#### 32-pin 8mm x 13.4mm sTSP Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.465 ±0.008	11.80 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.02 ±0.008	0.50 ±0.20
L1		0.031 ±0.005	0.8 ±0.125
y		0.003 (MAX)	0.076 (MAX)
Θ		0°~5°	0°~5°

#### 36-ball 6mm × 8mm TFBGA Package Outline Dimension



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	0.94	—	—	0.037
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (450mil) SOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BSL-45SL
				Tape Reel	LY62L2568BSL-45SLT
			-40°C~85°C	Tray	LY62L2568BSL-45SLI
				Tape Reel	LY62L2568BSL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BSL-55SL
				Tape Reel	LY62L2568BSL-55SLT
-40°C~85°C			Tray	LY62L2568BSL-55SLI	
			Tape Reel	LY62L2568BSL-55SLIT	



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (600mil) PDIP	45	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568BPL-45SL
			-40°C~85°C	Tube	LY62L2568BPL-45SLI
	55	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568BPL-55SL
			-40°C~85°C	Tube	LY62L2568BPL-55SLI





#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 20mm) TSOP I	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BLL-45SL
				Tape Reel	LY62L2568BLL-45SLT
			-40°C~85°C	Tray	LY62L2568BLL-45SLI
				Tape Reel	LY62L2568BLL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BLL-55SL
				Tape Reel	LY62L2568BLL-55SLT
-40°C~85°C			Tray	LY62L2568BLL-55SLI	
			Tape Reel	LY62L2568BLL-55SLIT	



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 13.4mm) sTSOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BRL-45SL
				Tape Reel	LY62L2568BRL-45SLT
			-40°C~85°C	Tray	LY62L2568BRL-45SLI
				Tape Reel	LY62L2568BRL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BRL-55SL
				Tape Reel	LY62L2568BRL-55SLT
-40°C~85°C			Tray	LY62L2568BRL-55SLI	
			Tape Reel	LY62L2568BRL-55SLIT	



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
36-ball (6mm x 8mm) TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BGL-45SL
				Tape Reel	LY62L2568BGL-45SLT
			-40°C~85°C	Tray	LY62L2568BGL-45SLI
				Tape Reel	LY62L2568BGL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568BGL-55SL
				Tape Reel	LY62L2568BGL-55SLT
			-40°C~85°C	Tray	LY62L2568BGL-55SLI
				Tape Reel	LY62L2568BGL-55SLIT



**Lyontek Inc.**

**LY62L2568B**

Rev. 1.2

**256K X 8 BIT LOW POWER CMOS SRAM**

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