



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jan.10.2008
Rev. 1.1	Added I _{SB} Spec.	Feb.1.2008
Rev. 1.2	Revised I _{CC1} /I _{SB1} /V _{DR} /I _{DR} Spec.	Mar.2.2009
Rev. 1.3	Revised V _{TERM} to V _{T1} and V _{T2} Revised Test Condition of I _{SB1} /I _{DR} Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS Revised PACKAGE OUTLINE DIMENSION in page 11 Revised V _{IH} to 0.7*V _{CC}	May.7.2010
Rev. 1.4	Revised ORDERING INFORMATION in page 11	Aug.25.2010
Rev. 1.5	Deleted E grade Added SL grade Revised V _{IH} in page 3	Apr.25.2011
Rev. 1.6	Revised TEST CONDITION of V _{IH} in page 4	May.13.2011
Rev. 1.7	Revised PACKAGE OUTLINE DIMENSION in page 10	Jul.27.2011
Rev. 1.8	Deleted WRITE CYCLE Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions in page 7	Jun.29.2016
Rev. 1.9	Added Notes:5 in DC ELECTRICAL CHARACTERISTICS (page4).	Sep.21.2016
Rev. 2.0	1. Deleted FEATURES Standby current : 3μA (TYP.) SL-version--Page 1 2. Deleted PRODUCT FAMILY Standby(I _{SB1} ,TYP.) :3μA(SL) --- Page 1 3. Deleted DC ELECTRICAL CHARACTERISTICS : Standby Power Supply Current : I _{SB1} --- Page4 4. Deleted DC ELECTRICAL CHARACTERISTICS : Notes: 5--- Page 4 5. Deleted DATA RETENTION CHARACTERISTICS : Data Retention Current: I _{DR} --- Page 8 6. Revised ORDERING INFORMATION in Page 11~Page14	Jun.18.2024

FEATURES

- Fast access time : 55/70ns
- Low power consumption:
Operating current : 30/20mA (TYP.)
Standby current : 6 μ A (TYP.) LL-version
- Single 2.7V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62W10248 is a 8,388,608-bit low power CMOS static random access memory organized as 1,048,576 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

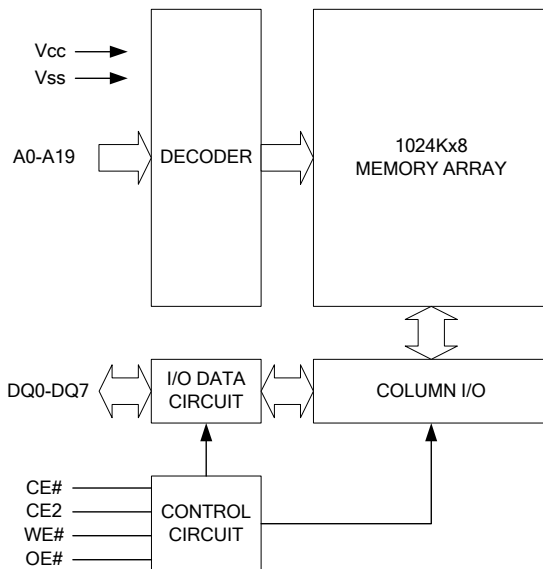
The LY62W10248 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W10248 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62W10248	0 ~ 70°C	2.7 ~ 5.5V	55/70ns	6 μ A(LL)	30/20mA
LY62W10248(I)	-40 ~ 85°C	2.7 ~ 5.5V	55/70ns	6 μ A(LL)	30/20mA

FUNCTIONAL BLOCK DIAGRAM

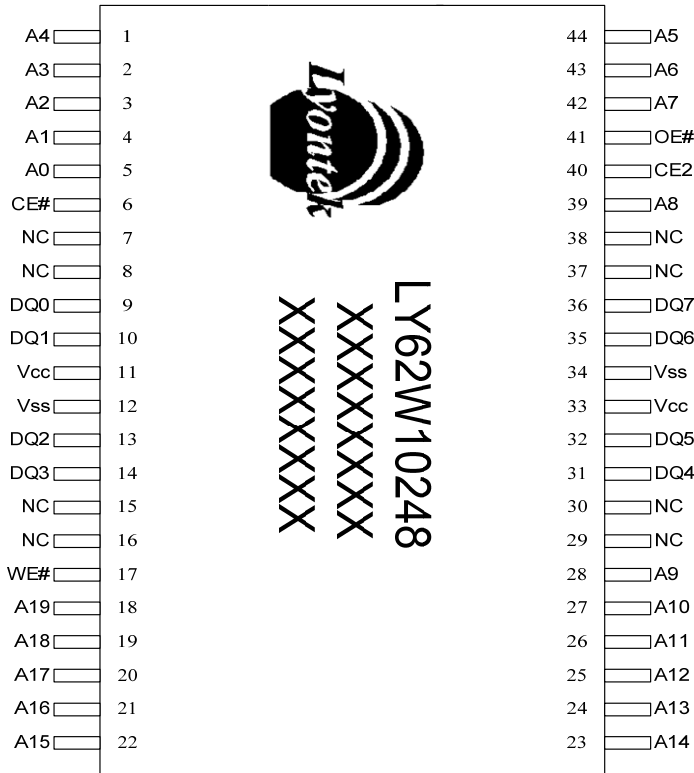


PIN DESCRIPTION

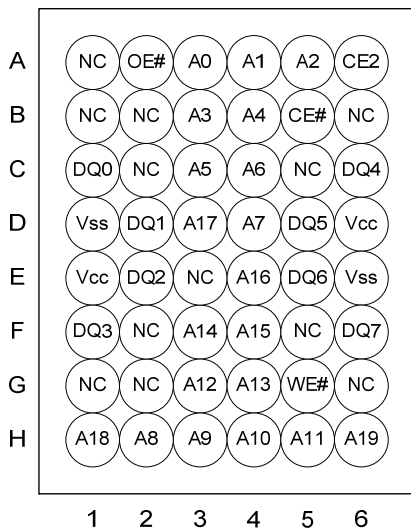
SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



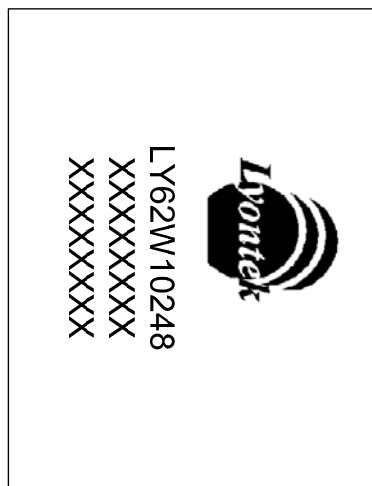
PIN CONFIGURATION



TSOP-II



TFPGA(See through with Top View)



TFPGA(Top View)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB}, I_{SB1}
	X	L	X	X	High-Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC}, I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*4	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.0	5.5	V	
Input High Voltage	V _{IH} *1	V _{CC} = 2.7 ~ 3.6V	2.2	-	V _{CC} +0.5	V	
		V _{CC} = 4.5 ~ 5.5V	2.4	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} *2		- 0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	- 55	-	30	60	mA
			- 70	-	20	50	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	4	12	mA	
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Other pins at V _{IL} or V _{IH}	-	0.15	2	mA	
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	6	30	μA
			LLI	-	6	50	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

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AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W10248-55		LY62W10248-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns

(2) WRITE CYCLE

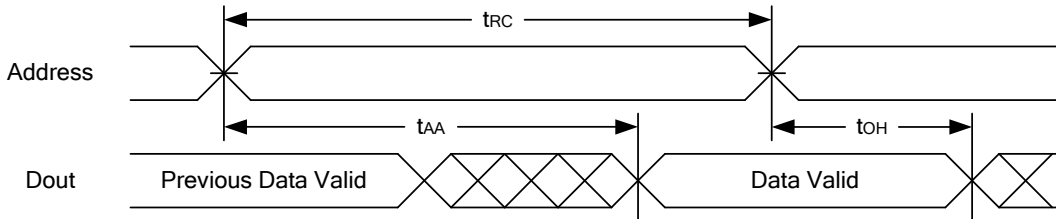
PARAMETER	SYM.	LY62W10248-55		LY62W10248-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

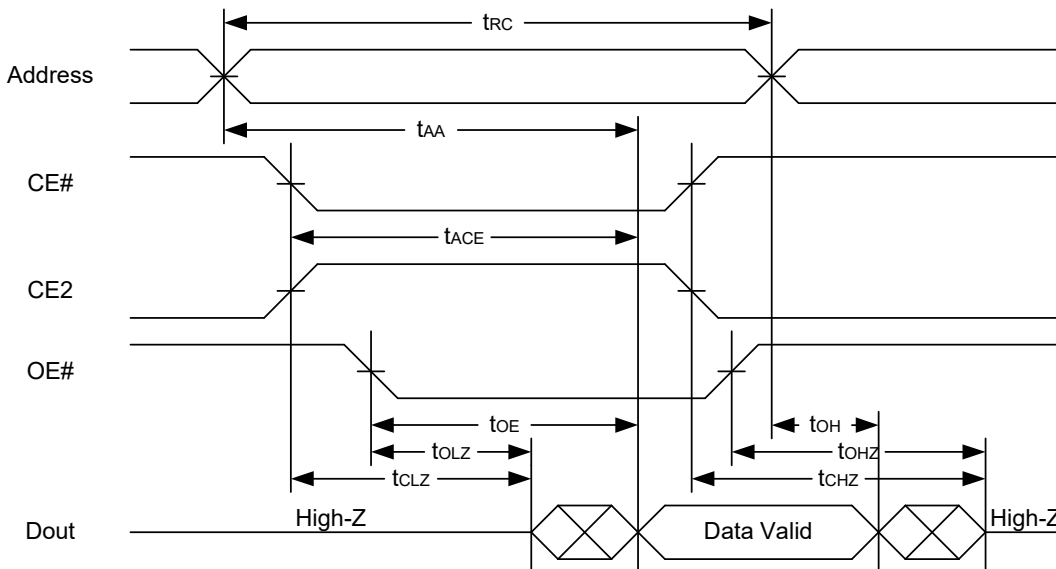


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

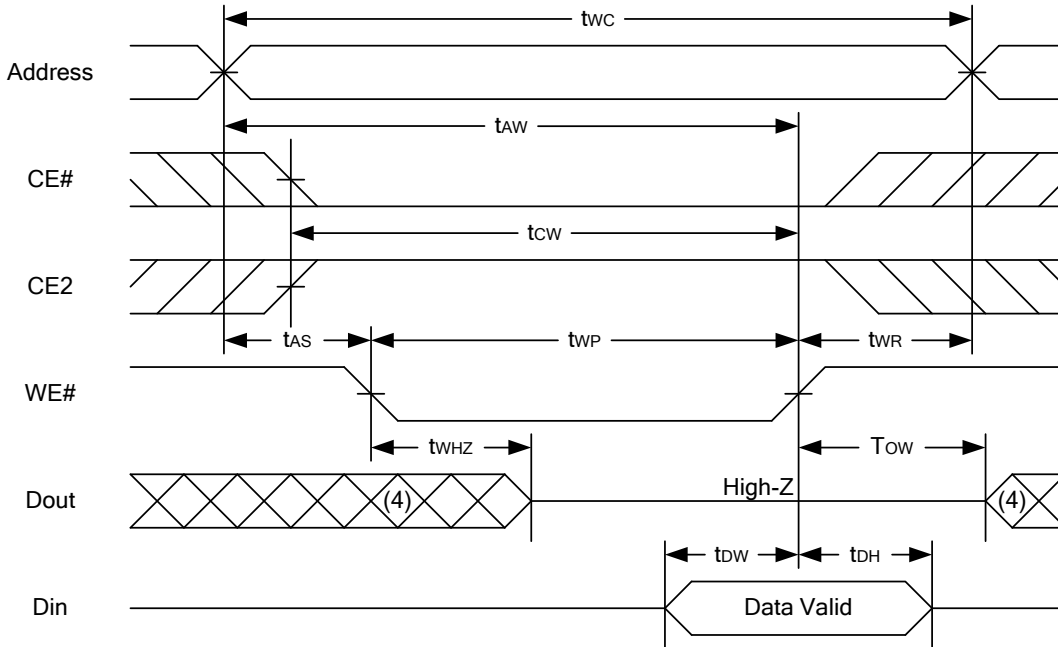


Notes :

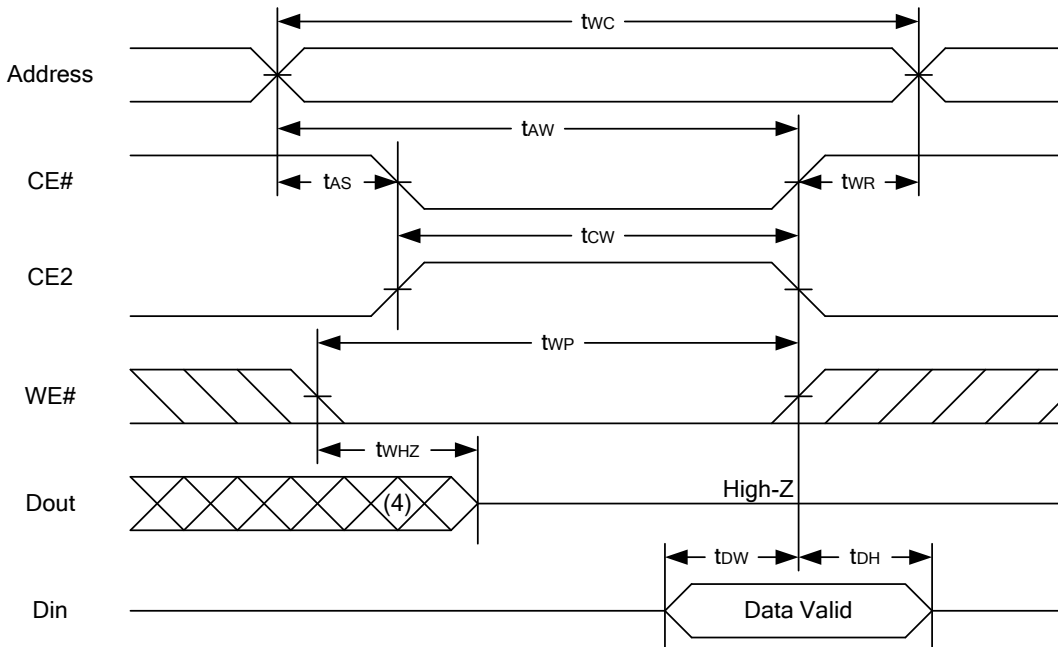
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{wp} must be greater than t_{whz} + t_{dw} to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{ow} and t_{whz} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

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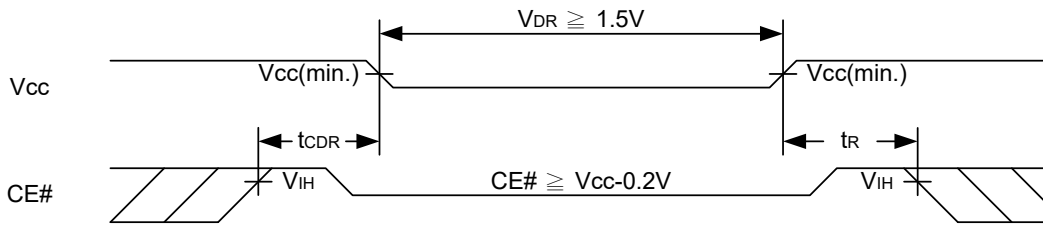
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	4	30	μA
			LLI	-	4	50	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC} *	-	-	ns	

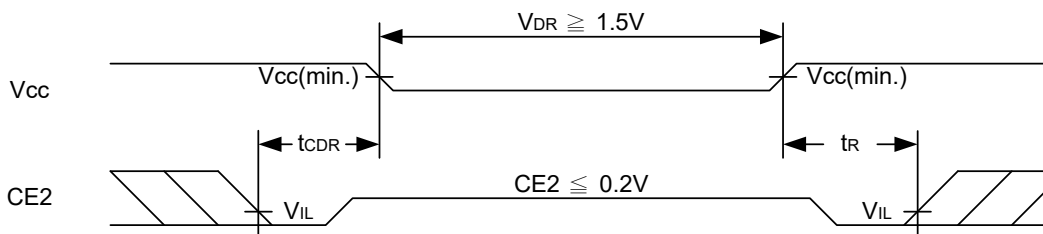
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



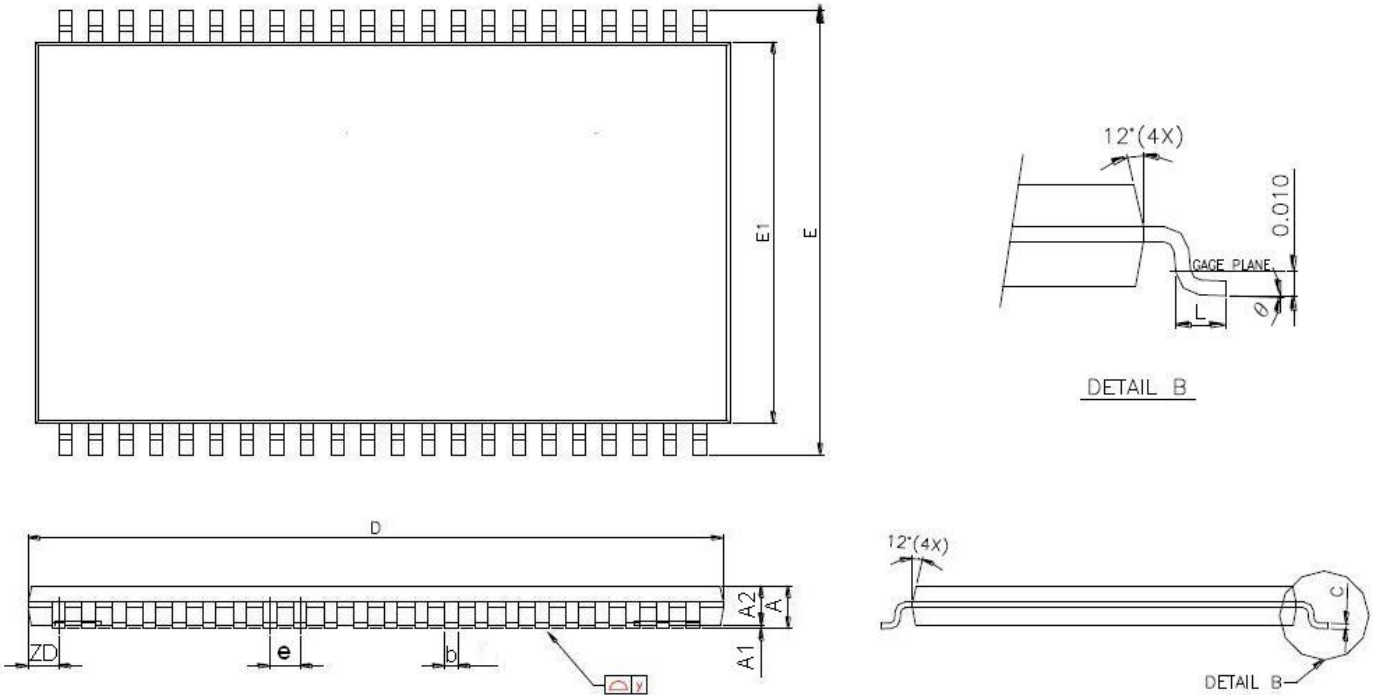
Low V_{CC} Data Retention Waveform (2) (CE2 controlled)





PACKAGE OUTLINE DIMENSION

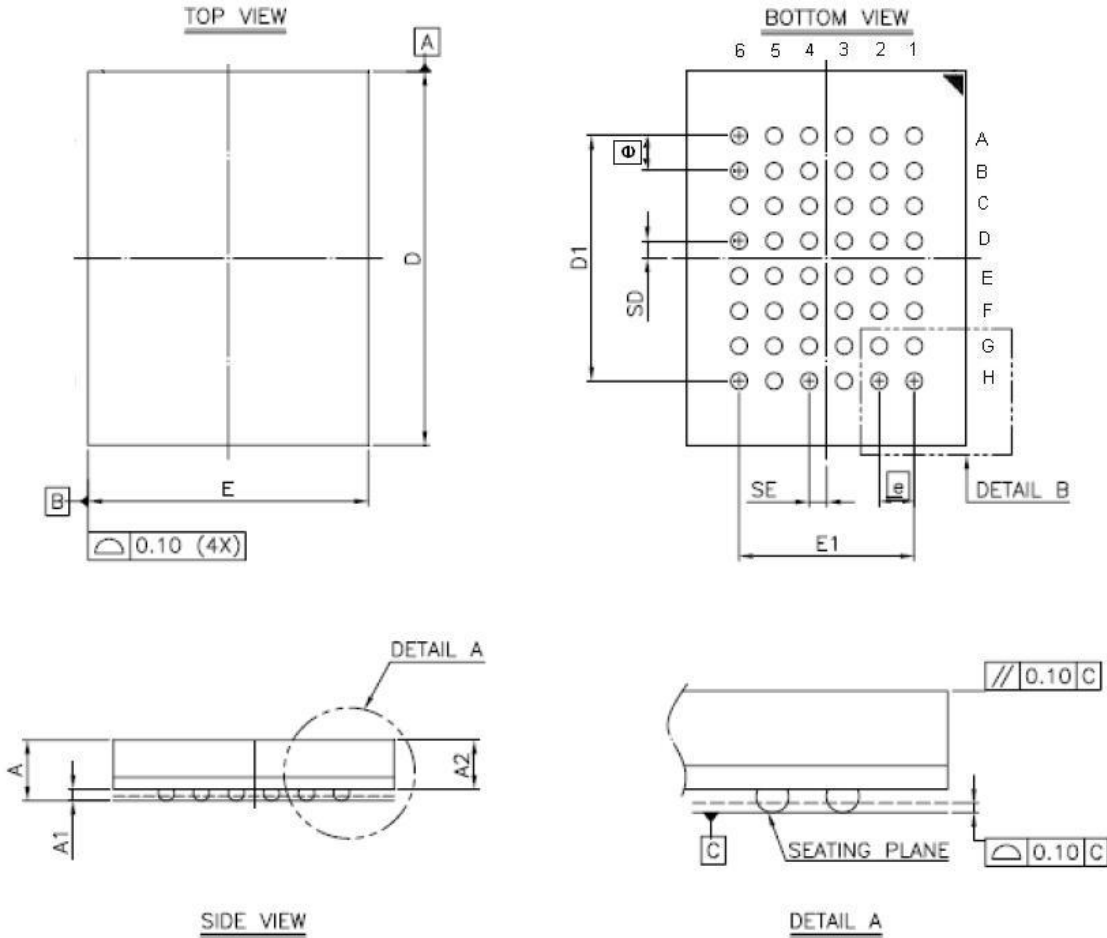
44-pin 400mil TSOP-II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

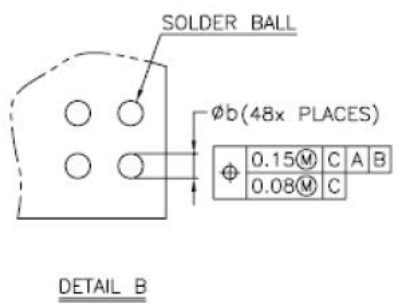


48-ball 6mm × 8mm TFBGA Package Outline Dimension



SIDE VIEW

DETAIL A



DETAIL B

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

- NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. REFERENCE DOCUMENT : JEDEC MO-207.



ORDERING INFORMATION

[Production Status: M/P]

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44Pin (400mil) TSOP-II	55	Ultra Low Power	0°C~70°C	Tray	LY62W10248ML-55LL
				Tape Reel	LY62W10248ML-55LLT
			-40°C~85°C	Tray	LY62W10248ML-55LLI
				Tape Reel	LY62W10248ML-55LLIT
	70	Ultra Low Power	0°C~70°C	Tray	LY62W10248ML-70LL
				Tape Reel	LY62W10248ML-70LLT
			-40°C~85°C	Tray	LY62W10248ML-70LLI
				Tape Reel	LY62W10248ML-70LLIT



ORDERING INFORMATION

[Production Status: M/P]

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-ball (6mmx8mm) TFBGA	55	Ultra Low Power	0°C~70°C	Tray	LY62W10248GL-55LL
				Tape Reel	LY62W10248GL-55LLT
			-40°C~85°C	Tray	LY62W10248GL-55LLI
				Tape Reel	LY62W10248GL-55LLIT
	70	Ultra Low Power	0°C~70°C	Tray	LY62W10248GL-70LL
				Tape Reel	LY62W10248GL-70LLT
			-40°C~85°C	Tray	LY62W10248GL-70LLI
				Tape Reel	LY62W10248GL-70LLIT



ORDERING INFORMATION

[Production Status: **EOL**]

Power Type : Special Ultra Low Power

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	EOL Item No.	Substitute Product
44Pin (400mil) TSOP-II	55	0°C~70°C	Tray	LY62W10248ML-55SL	LY62W10248BML-45SL
			Tape Reel	LY62W10248ML-55SLT	LY62W10248BML-45SLT
		-40°C~85°C	Tray	LY62W10248ML-55SLI	LY62W10248BML-45SLI
			Tape Reel	LY62W10248ML-55SLIT	LY62W10248BML-45SLIT
	70	0°C~70°C	Tray	LY62W10248ML-70SL	LY62W10248BML-45SL
			Tape Reel	LY62W10248ML-70SLT	LY62W10248BML-45SLT
		-40°C~85°C	Tray	LY62W10248ML-70SLI	LY62W10248BML-45SLI
			Tape Reel	LY62W10248ML-70SLIT	LY62W10248BML-45SLIT



ORDERING INFORMATION

[Production Status: **EOL**]

Power Type : Special Ultra Low Power

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	EOL Item No.	Substitute Product
48-ball (6mmx8mm) TFBGA	55	0°C~70°C	Tray	LY62W10248GL-55SL	LY62W10248GL-55SL
			Tape Reel	LY62W10248GL-55SLT	LY62W10248GL-55SLT
		-40°C~85°C	Tray	LY62W10248GL-55SLI	LY62W10248GL-55SLI
			Tape Reel	LY62W10248GL-55SLIT	LY62W10248GL-55SLIT
	70	0°C~70°C	Tray	LY62W10248GL-70SL	LY62W10248GL-70SL
			Tape Reel	LY62W10248GL-70SLT	LY62W10248GL-70SLT
		-40°C~85°C	Tray	LY62W10248GL-70SLI	LY62W10248GL-70SLI
			Tape Reel	LY62W10248GL-70SLIT	LY62W10248GL-70SLIT



Lyontek Inc.

LY62W10248

Rev. 2.0

1024K X 8 BIT LOW POWER CMOS SRAM

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