



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Aug.1.2007
Rev. 1.1	Revised V_{IH} to TTL compatible	Jan.9.2008
Rev. 1.2	Revised I_{DR} (TYP.)	Feb.22.2008
Rev. 1.3	Revised V_{IH} to $0.7 \cdot V_{CC}$	May.6.2008
Rev. 1.4	Revised V_{DR}	Mar.3.2009
Rev. 1.5	Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Deleted T_{SOLDER} in ABSOLUTE MAXIMUM RATINGS Revised PACKAGE OUTLINE DIMENSION in page9/10/12/13	May.6.2010
Rev. 1.6	Revised ORDERING INFORMATION in page 14	Aug.30.2010
Rev. 1.7	Added SL Grade Deleted E Grade Revised I_{SB1}/I_{DR}	Aug.9.2011
Rev. 1.8	Deleted WRITE CYCLE Notes : 1.WE#, CE# must be high or CE2 must be low during all address transitions in page 7	Jun.29.2016
Rev. 1.9	Removed Package Type : PDIP/BGA	Apr.08. 2019
Rev. 1.10	Revised ORDERING INFORMATION in page 11 32 Pin(450mil) SOP PackingType : Tube→Tray	Aug.24.2023

FEATURES

- Fast access time : 55/70ns
- Low power consumption:
Operating current : 20/18mA (TYP.)
Standby current : 1 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450 mil SOP
32-pin 8mm x 20mm TSOP I
32-pin 8mm x 13.4mm sTSP

GENERAL DESCRIPTION

The LY62W2568 is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

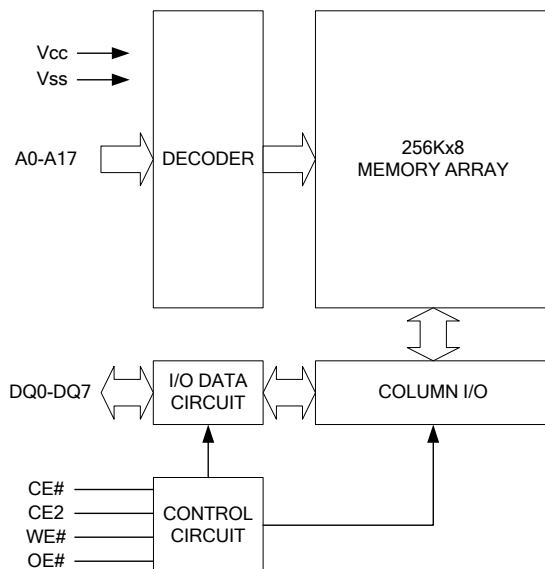
The LY62W2568 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W2568 operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(Isb1,TYP.)	Operating(Icc,TYP.)
LY62W2568	0 ~ 70°C	2.7 ~ 5.5V	55/70ns	1 μ A	20/18mA
LY62W2568(I)	-40 ~ 85°C	2.7 ~ 5.5V	55/70ns	1 μ A	20/18mA

FUNCTIONAL BLOCK DIAGRAM

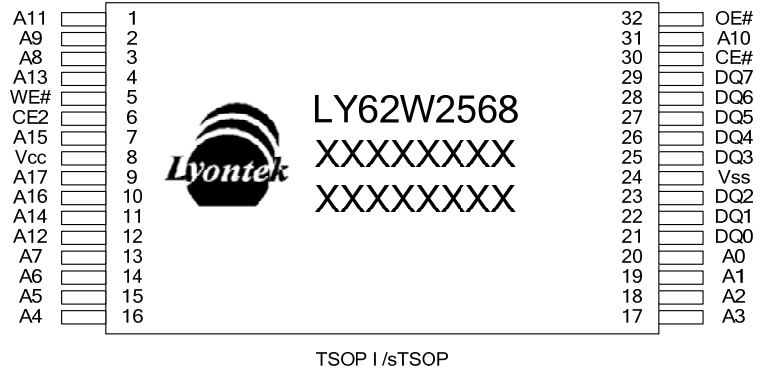
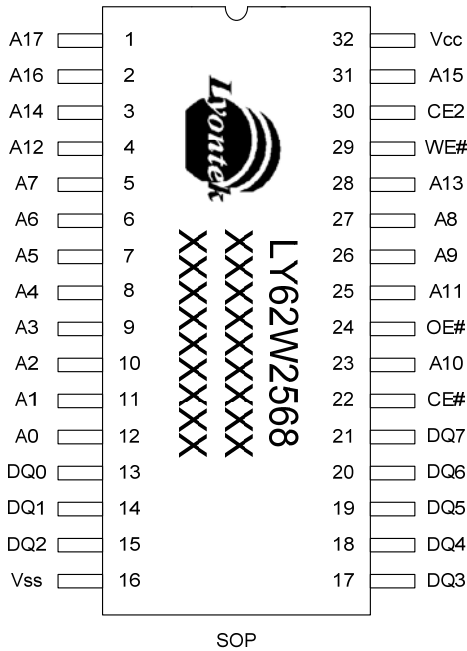


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to V _{cc} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{cc} , I _{cc1}
Read	L	H	L	H	D _{OUT}	I _{cc} , I _{cc1}
Write	L	H	X	L	D _{IN}	I _{cc} , I _{cc1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*4	MAX.	UNIT		
Supply Voltage	V _{CC}		2.7	3.0	5.5	V		
Input High Voltage	V _{IH} *1		0.7*V _{CC}	-	V _{CC} +0.3	V		
Input Low Voltage	V _{IL} *2		- 0.2	-	0.6	V		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA		
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA		
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	2.7	-	V		
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	- 55	-	20	60	mA	
			- 70	-	18	50	mA	
	I _{CC1}	Cycle time = 1μs CE# = 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} - 0.2V	-	4	10	mA		
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} - 0.2V	LL/LLI	-	1	50	μA	
			SL*5	25°C	-	1	5	μA
			SLI*5	40°C	-	1	5	μA
			SL	-	1	20	μA	
			SLI	-	1	25	μA	

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -2mA/4mA

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2F, No.17, Industry E. Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan.

TEL: 886-3-6668838

FAX: 886-3-6668836



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W2568-55		LY62W2568-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns

(2) WRITE CYCLE

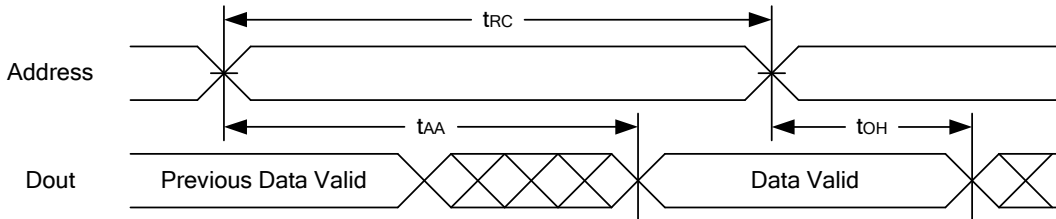
PARAMETER	SYM.	LY62W2568-55		LY62W2568-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

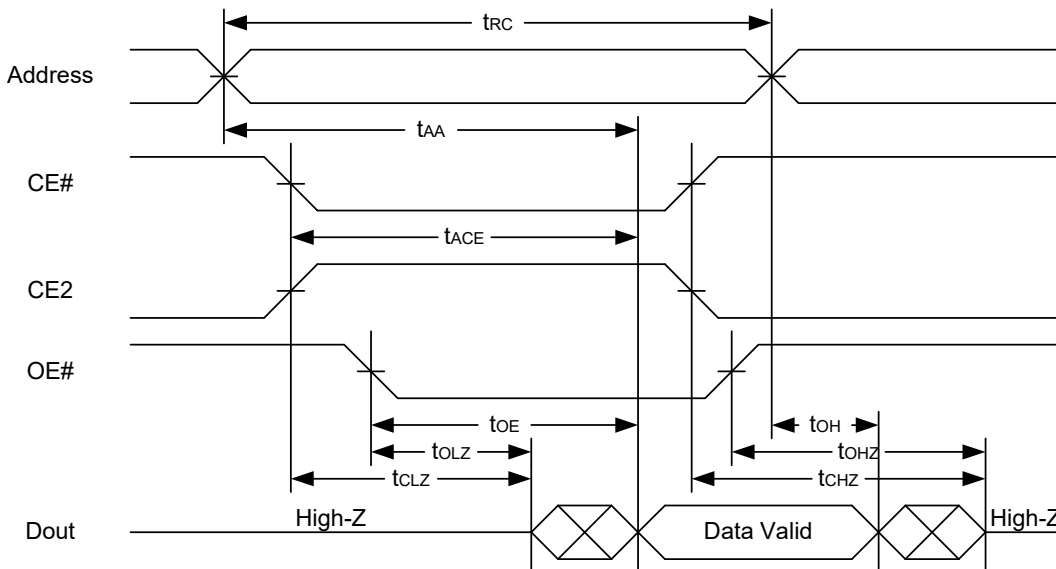


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

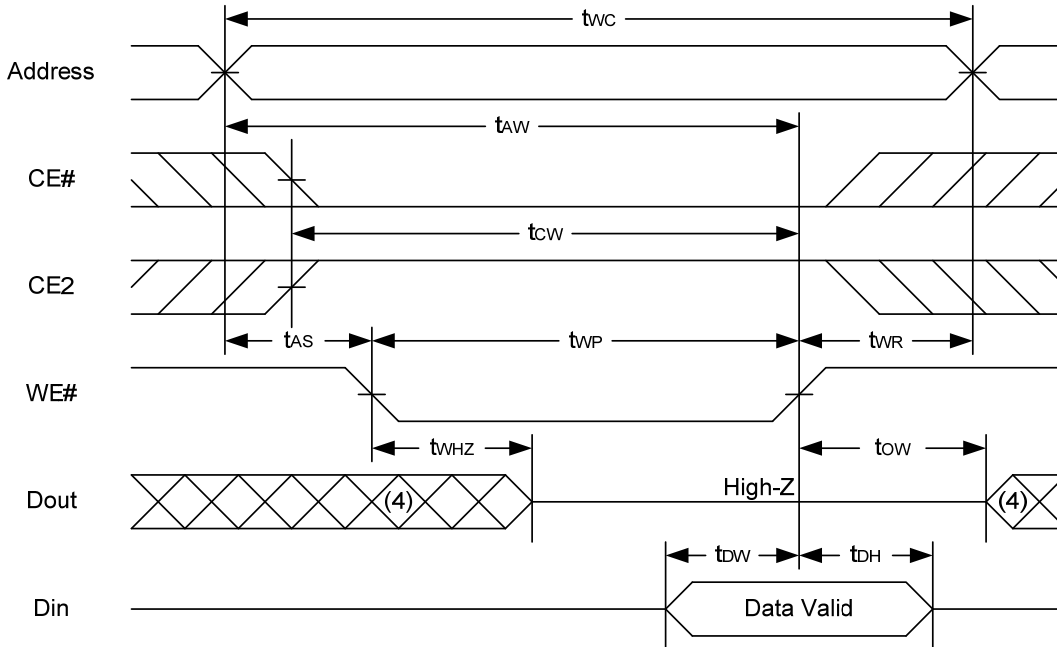


Notes :

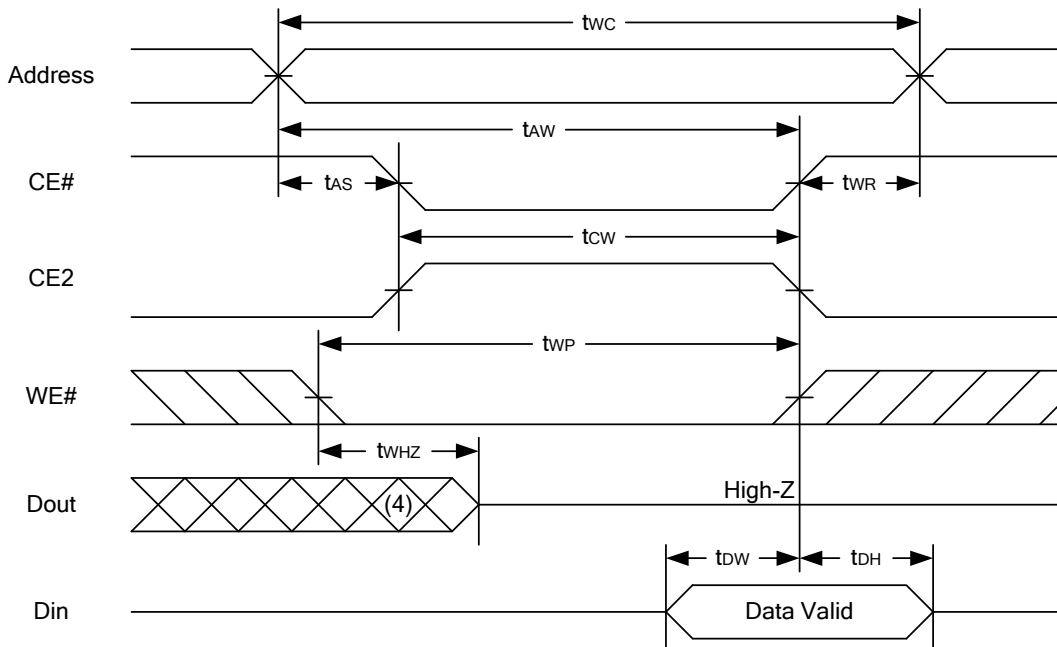
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OH} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OH} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE#-controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

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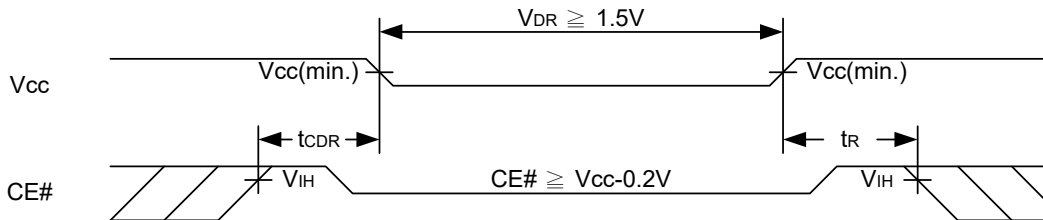
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL/LLI	-	0.5	20	μA
			SL 25°C	-	0.5	4	μA
			SLI 40°C	-	0.5	4	μA
			SL/SLI	-	0.5	15	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC} *	-	-	ns	

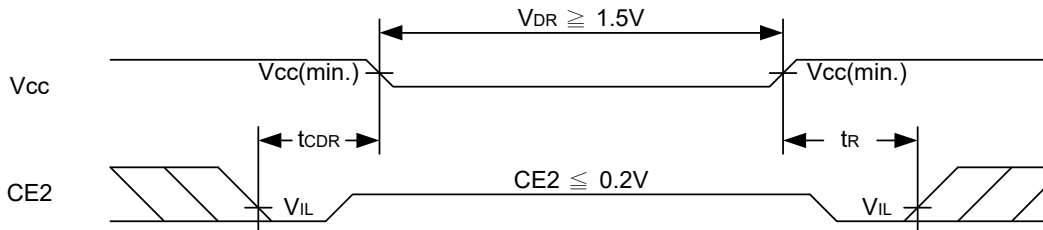
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



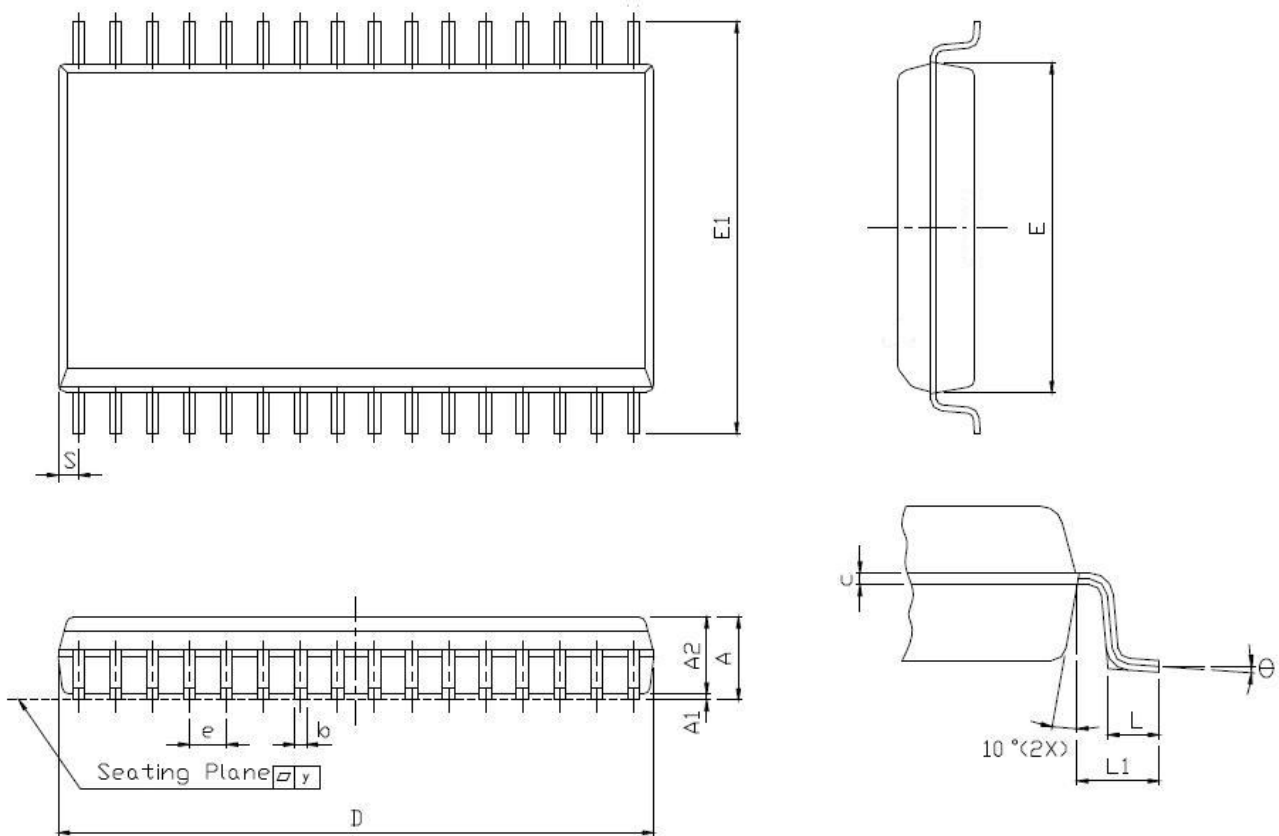
Low V_{CC} Data Retention Waveform (2) (CE2 controlled)





PACKAGE OUTLINE DIMENSION

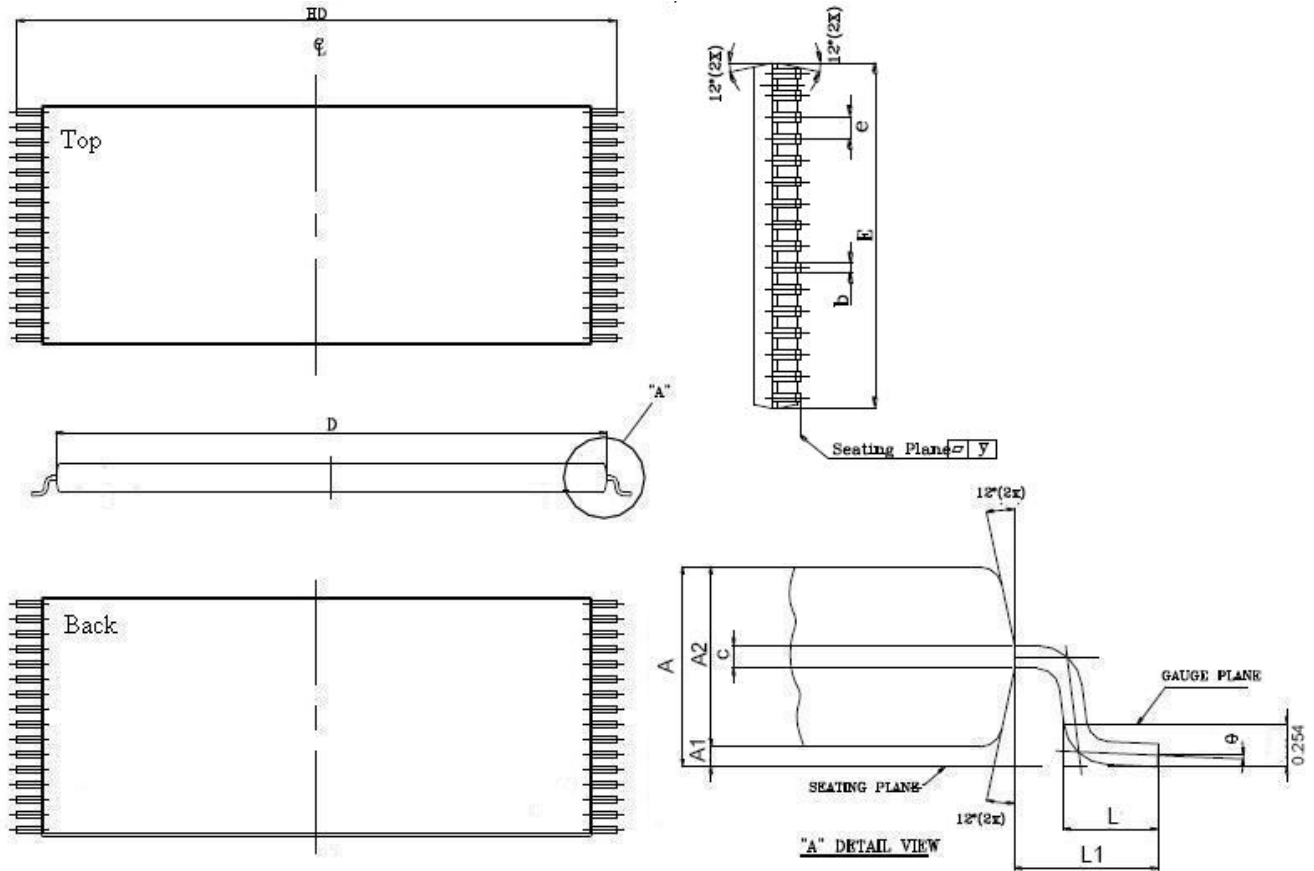
32 pin 450 mil SOP Package Outline Dimension



SYM.	UNIT	INCH.(BASE)	MM(REF)
	A		0.120(MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.116(MAX)	2.946(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445±0.006	11.303±0.152
E1		0.555±0.025	14.097±0.635
e		0.050(TYP)	1.270(TYP)
L		0.033±0.017	0.838±0.432
L1		0.055±0.008	1.397±0.203
S		0.026(MAX)	0.660(MAX)
y		0.004(MAX)	0.101(MAX)
Θ		0° -10°	0° -10°



32 pin 8mm x 20mm TSOP I Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.724 ±0.008	18.40 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.024 ±0.004	0.60 ±0.10
L1		0.0315 ±0.004	0.08 ±0.10
y		0.003 (MAX)	0.08 (MAX)
∅		0°~5°	0°~5°



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin(450mil) SOP	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568SL-55SL
				Tape Reel	LY62W2568SL-55SLT
			-40°C~85°C	Tray	LY62W2568SL-55SLI
				Tape Reel	LY62W2568SL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62W2568SL-55LL
				Tape Reel	LY62W2568SL-55LLT
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568SL-70SL
				Tape Reel	LY62W2568SL-70SLT
			-40°C~85°C	Tray	LY62W2568SL-70SLI
				Tape Reel	LY62W2568SL-70SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62W2568SL-70LL
				Tape Reel	LY62W2568SL-70LLT
	-40°C~85°C	Tray	LY62W2568SL-70LLI		
		Tape Reel	LY62W2568SL-70LLIT		



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin (8mmx20mm) TSOP I	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568LL-55SL
				Tape Reel	LY62W2568LL-55SLT
			-40°C~85°C	Tray	LY62W2568LL-55SLI
				Tape Reel	LY62W2568LL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62W2568LL-55LL
				Tape Reel	LY62W2568LL-55LLT
		-40°C~85°C	Tray	LY62W2568LL-55LLI	
			Tape Reel	LY62W2568LL-55LLIT	
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568LL-70SL
				Tape Reel	LY62W2568LL-70SLT
			-40°C~85°C	Tray	LY62W2568LL-70SLI
				Tape Reel	LY62W2568LL-70SLIT
Ultra Low Power		0°C~70°C	Tray	LY62W2568LL-70LL	
			Tape Reel	LY62W2568LL-70LLT	
	-40°C~85°C	Tray	LY62W2568LL-70LLI		
		Tape Reel	LY62W2568LL-70LLIT		



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin (8mmx13.4mm) sTSSOP	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568RL-55SL
				Tape Reel	LY62W2568RL-55SLT
			-40°C~85°C	Tray	LY62W2568RL-55SLI
				Tape Reel	LY62W2568RL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62W2568RL-55LL
				Tape Reel	LY62W2568RL-55LLT
		-40°C~85°C	Tray	LY62W2568RL-55LLI	
			Tape Reel	LY62W2568RL-55LLIT	
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568RL-70SL
				Tape Reel	LY62W2568RL-70SLT
			-40°C~85°C	Tray	LY62W2568RL-70SLI
				Tape Reel	LY62W2568RL-70SLIT
Ultra Low Power		0°C~70°C	Tray	LY62W2568RL-70LL	
			Tape Reel	LY62W2568RL-70LLT	
	-40°C~85°C	Tray	LY62W2568RL-70LLI		
		Tape Reel	LY62W2568RL-70LLIT		



Lyontek Inc.

LY62W2568

Rev. 1.10

256K X 8 BIT LOW POWER CMOS SRAM

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