



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev.1.0	Initial Issue	Jan.30.2024
Rev.1.1	Revised <u>DC ELECTRICAL CHARACTERISTICS</u> :ICC TEST CONDITION & Deleted ISB SYMBOL-----Page3	Mar.27.2024

FEATURES

- Fast access time : 45/55ns
- Low power consumption:
Operating current : 12/10mA (TYP.)
Standby current : 3 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62W51216B is a 8,388,608-bit low power CMOS static random access memory organized as 524,288 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

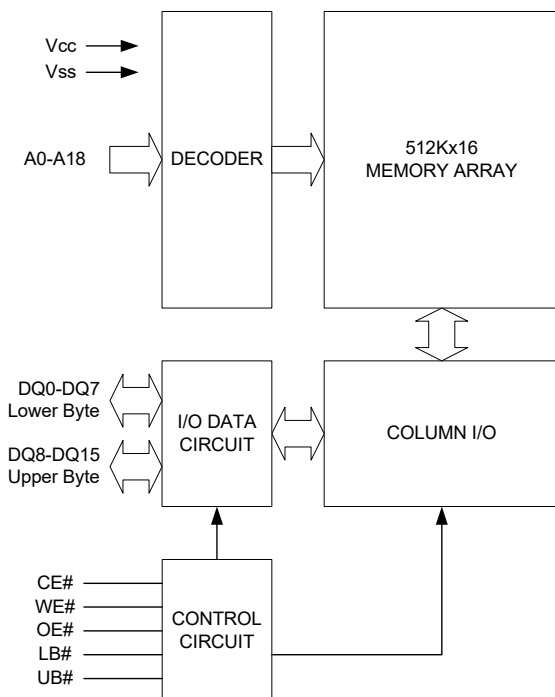
The LY62W51216B is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W51216B operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

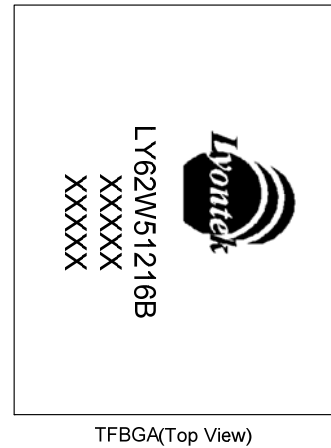
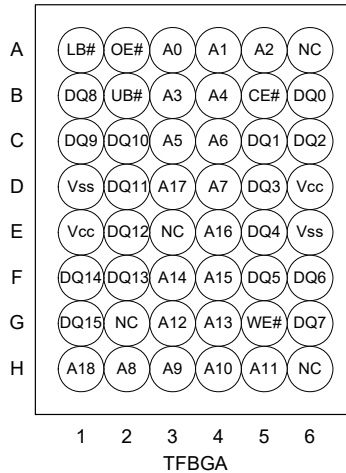
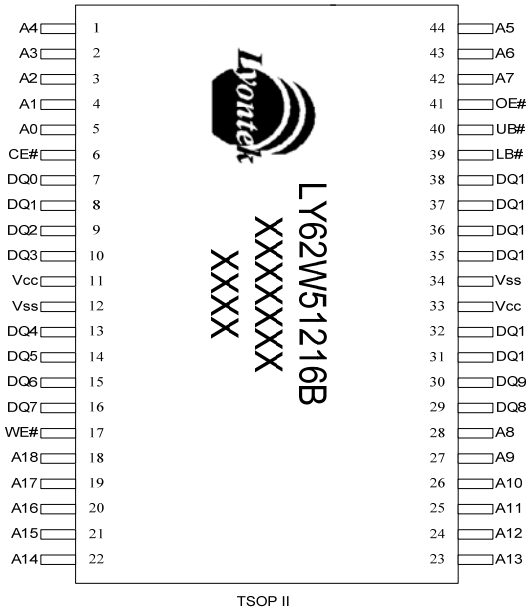
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(Isb1,TYP.)	Operating(Icc,TYP.)
LY62W51216B	0 ~ 70°C	2.7 ~ 5.5V	45/55ns	3 μ A	12/10mA
LY62W51216B(I)	-40 ~ 85°C	2.7 ~ 5.5V	45/55ns	3 μ A	12/10mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	L	X	High - Z	High - Z	I _{CC} , I _{CC1}
	L	H	H	X	L	High - Z	High - Z	
Read	L	L	H	L	H	D _{OUT}	High - Z	I _{CC} , I _{CC1}
	L	L	H	H	L	High - Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High - Z	I _{CC} , I _{CC1}
	L	X	L	H	L	High - Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.0	5.5	V	
Input High Voltage	V _{IH} ^{*1}	V _{CC} = 2.7 ~ 3.6V	2.2	-	V _{CC} +0.5	V	
		V _{CC} = 4.5 ~ 5.5V	2.4	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} ^{*2}	V _{CC} = 2.7 ~ 3.6V	-0.2	-	0.6	V	
		V _{CC} = 4.5 ~ 5.5V	-0.2	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# ≤ 0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-45	12	20	mA	
			-55	10	18	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	3	5	mA	
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V ; And Other pins at 0.2V or V _{CC} -0.2V	SL ^{*5}	25°C	3	8	μA
			SLI ^{*5}	40°C	4	10	μA
			SL		3	20	μA
			SLI		3	25	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

**CAPACITANCE (T_A = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

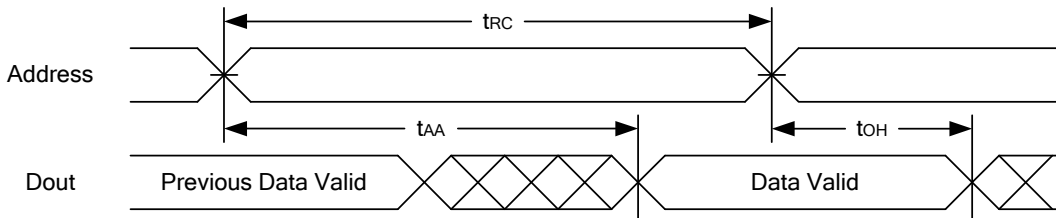
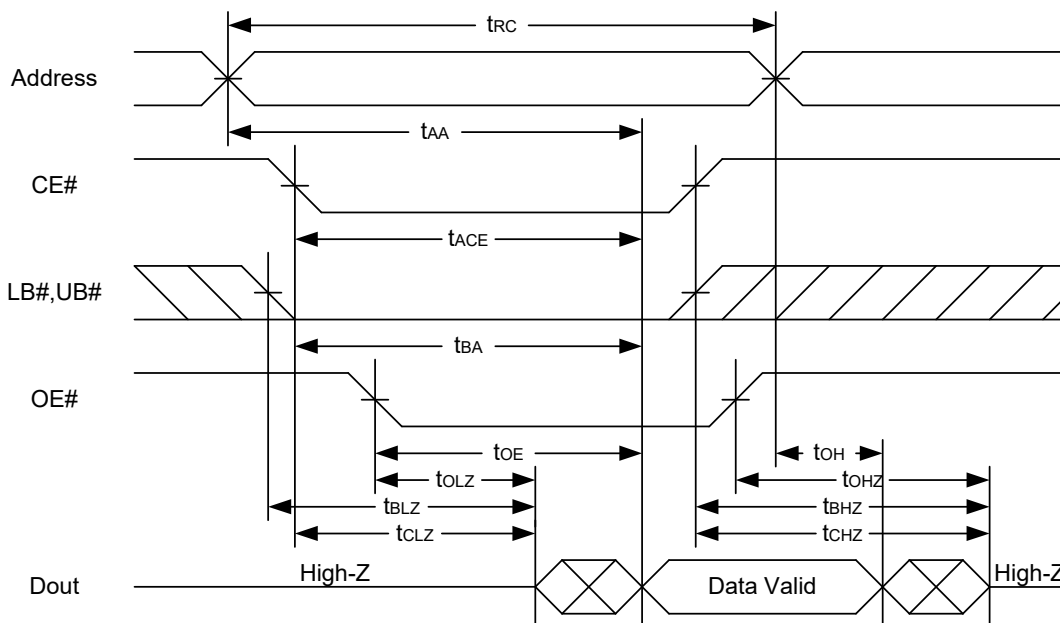
AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	LY62W51216B-45		LY62W51216B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	45	-	55	-	ns
Address Access Time	t _{AA}	-	45	-	55	ns
Chip Enable Access Time	t _{ACE}	-	45	-	55	ns
Output Enable Access Time	t _{OE}	-	25	-	30	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	2	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns
LB#, UB# Access Time	t _{BA}	-	45	-	55	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	15	-	25	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	10	-	10	-	ns

(2) WRITE CYCLE

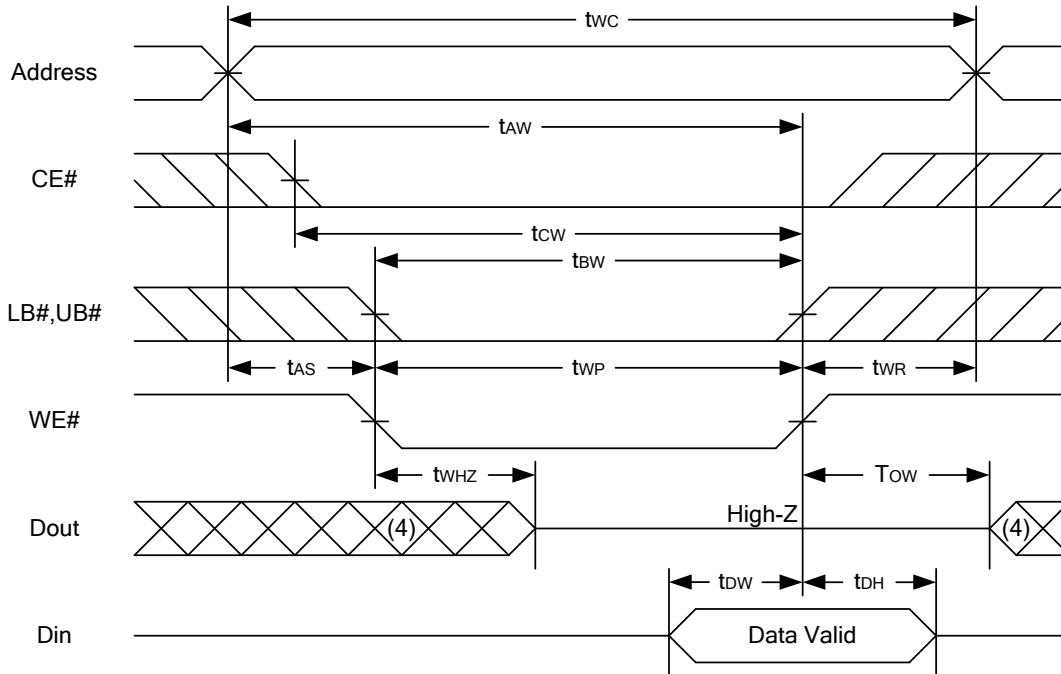
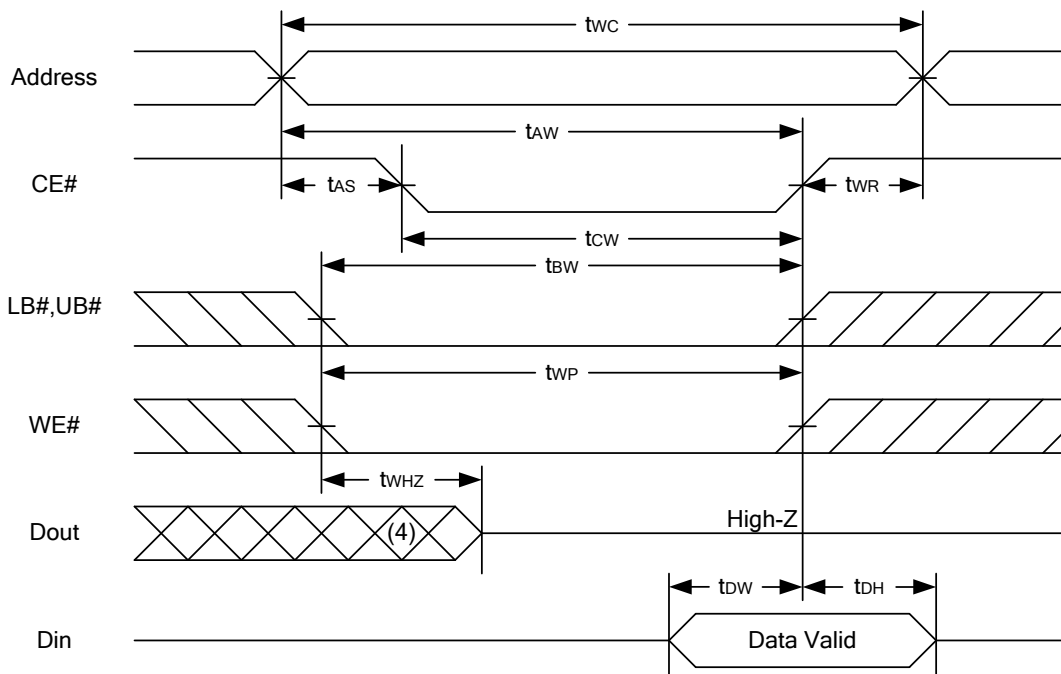
PARAMETER	SYM.	LY62W51216B-45		LY62W51216B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	45	-	55	-	ns
Address Valid to End of Write	t _{AW}	40	-	50	-	ns
Chip Enable to End of Write	t _{CW}	40	-	50	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	35	-	45	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	20	ns
LB#, UB# Valid to End of Write	t _{BW}	35	-	45	-	ns

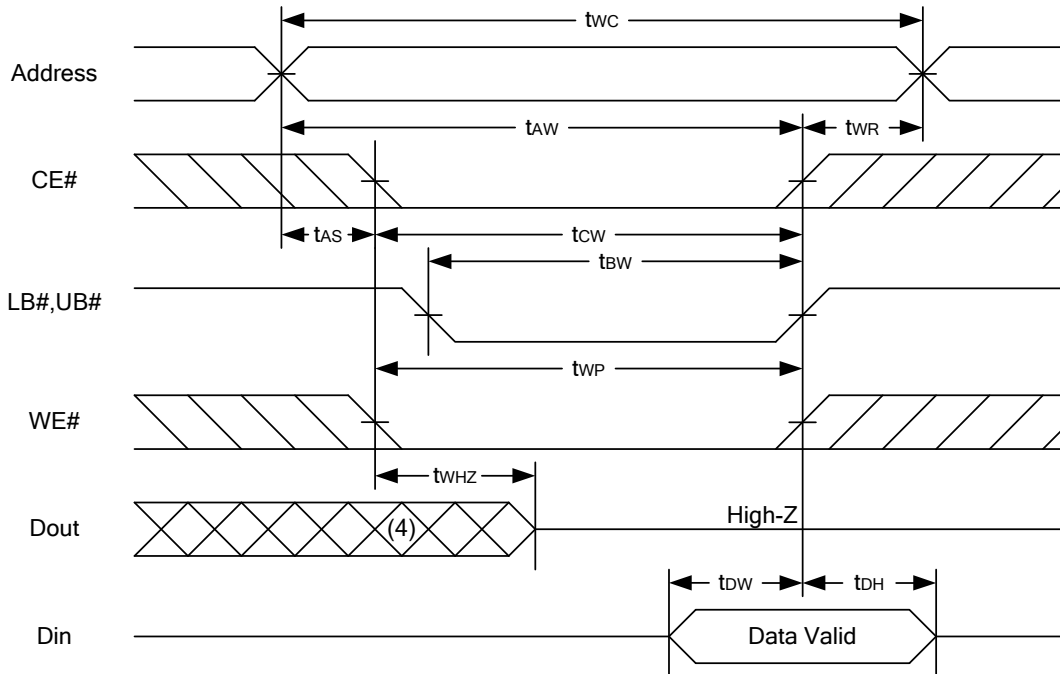
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS
READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)


Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OCHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OCHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

WRITE CYCLE 2 (CE# Controlled) (1,4,5)


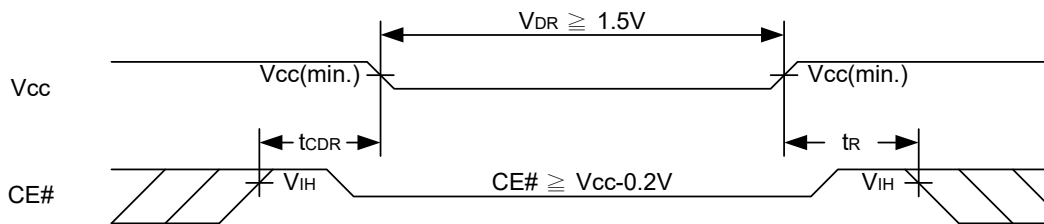
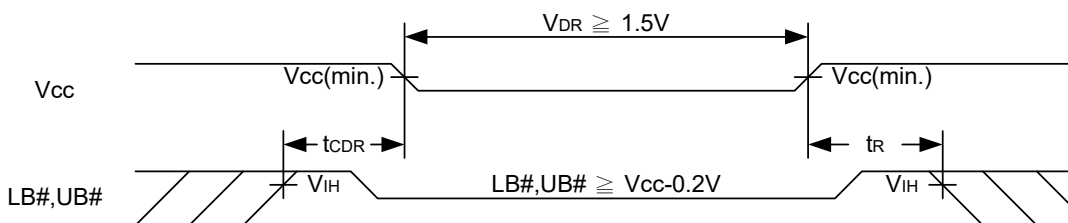
WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)

Notes :

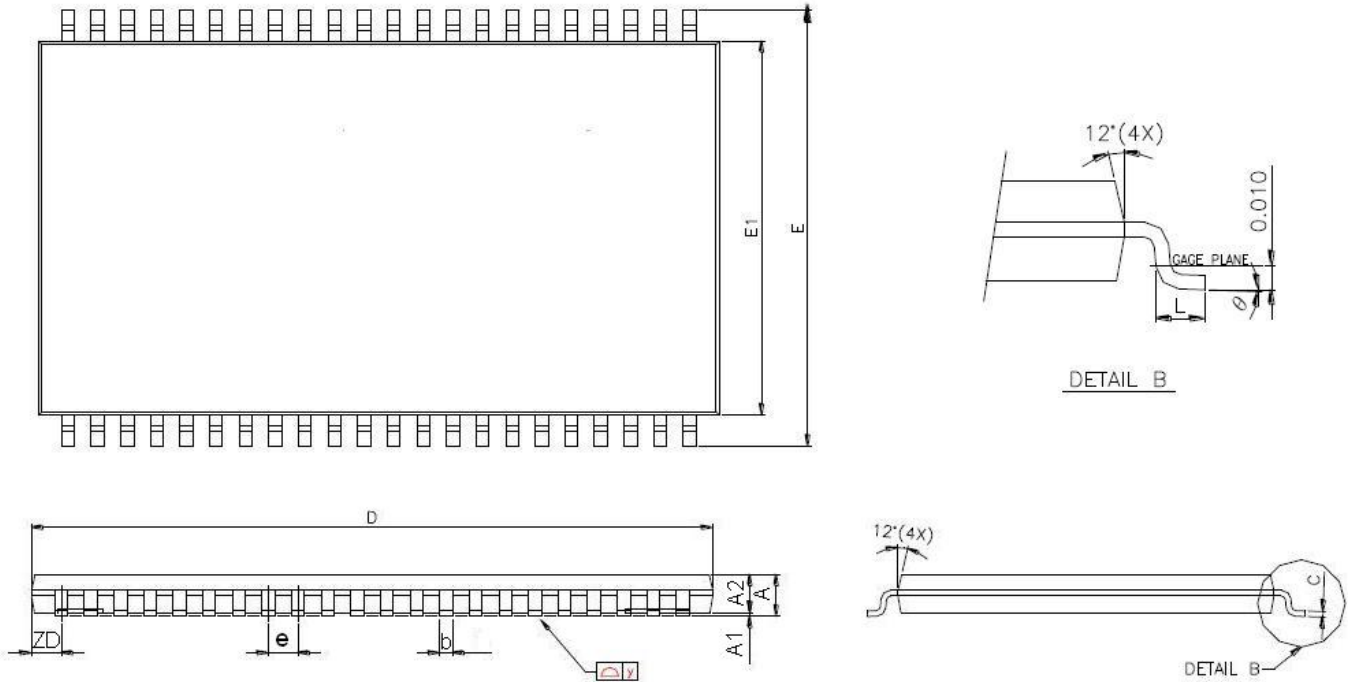
1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{BW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

DATA RETENTION CHARACTERISTICS

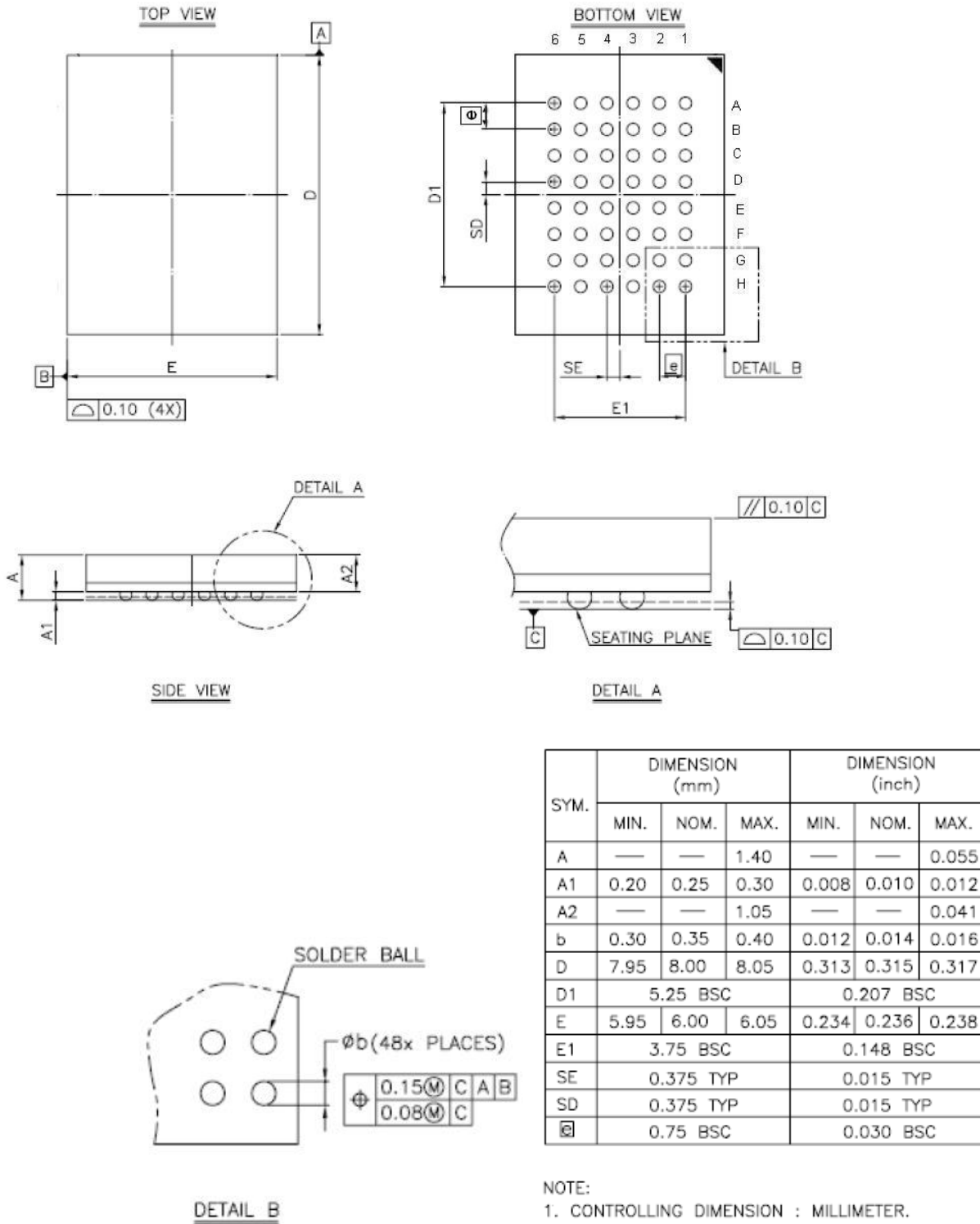
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Vcc for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	1.5	-	5.5	V		
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V Other pins at 0.2V or V _{CC} -0.2V	SL	25°C	-	3	8	μA
			SLI	40°C	-	4	10	μA
			SL		-	3	20	μA
			SLI		-	3	25	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM
Low Vcc Data Retention Waveform (1) (CE# controlled)

Low Vcc Data Retention Waveform (2) (LB#, UB# controlled)


PACKAGE OUTLINE DIMENSION
44-pin 400mil TSOP-II Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

48-ball 6mm × 8mm TFBGA Package Outline Dimension




ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44Pin 400mil TSOP-II	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BML-45SL
				Tape Reel	LY62W51216BML-45SLT
			-40°C~85°C	Tray	LY62W51216BML-45SLI
				Tape Reel	LY62W51216BML-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BML-55SL
				Tape Reel	LY62W51216BML-55SLT
			-40°C~85°C	Tray	LY62W51216BML-55SLI
				Tape Reel	LY62W51216BML-55SLIT
48-Ball 6mm x 8mm TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BGL-45SL
				Tape Reel	LY62W51216BGL-45SLT
			-40°C~85°C	Tray	LY62W51216BGL-45SLI
				Tape Reel	LY62W51216BGL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BGL-55SL
				Tape Reel	LY62W51216BGL-55SLT
			-40°C~85°C	Tray	LY62W51216BGL-55SLI
				Tape Reel	LY62W51216BGL-55SLIT



Lyontek Inc.

LY62W51216B

Rev. 1.1

512K X 16 BIT LOW POWER CMOS SRAM

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