



**Lyontek Inc.**

**LY69L6416A**

**64K X 16 BIT LOW POWER CMOS SRAM  
With Error-Correcting Code (ECC)**

Rev. 1.0

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**REVISION HISTORY**

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Mar.19.2020

### FEATURES

- Fast access time : 45/55ns
- Low power consumption:  
Operating current : 12/10mA (TYP.)  
Standby current : 1 $\mu$ A (TYP.)
- Single 2.7V ~ 3.6V power supply
- ECC : 1-bit error correction per byte
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400mil TSOP II  
48-ball 6mm\*8mm TFBGA

### GENERAL DESCRIPTION

The LY69L6416A is a 1,048,576-bit low power CMOS static random access memory organized as 65,536 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

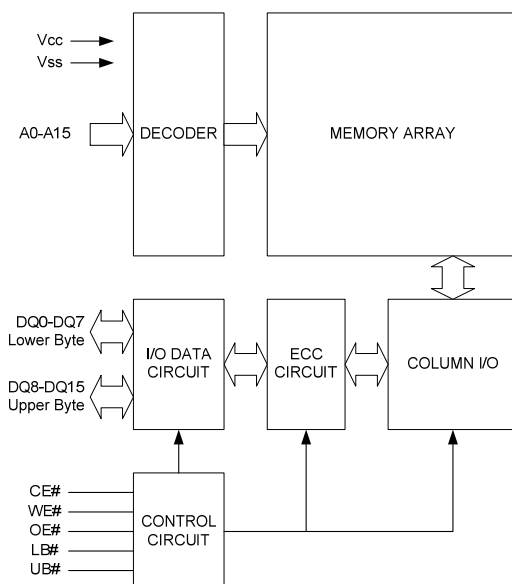
The LY69L6416A embeds error-correcting code (ECC) which can correct single-bit error per byte. It is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY69L6416A operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible.

### PRODUCT FAMILY

Product Family	Operating Temperature	V <sub>CC</sub> Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> , TYP.)	Operating(I <sub>CC</sub> , TYP.)
LY69L6416A	0 ~ 70°C	2.7 ~ 3.6V	45/55ns	1 $\mu$ A	12/10mA
LY69L6416A(I)	-40 ~ 85°C	2.7 ~ 3.6V	45/55ns	1 $\mu$ A	12/10mA

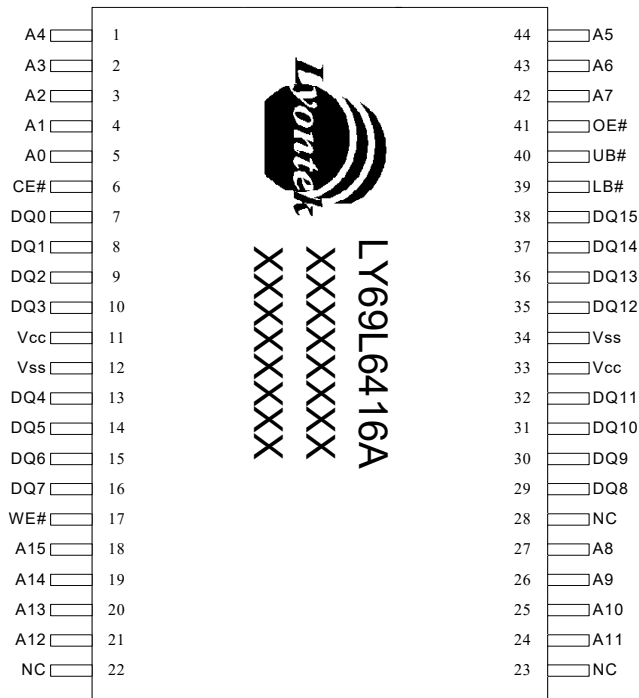
### FUNCTIONAL BLOCK DIAGRAM



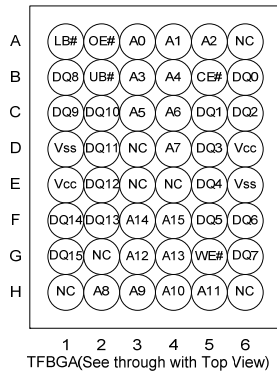
### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

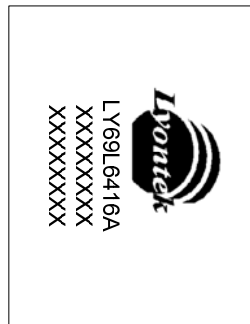
### PIN CONFIGURATION



TSOP II



TFPGA(See through with Top View)



TFPGA(Top View)



#### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on $V_{CC}$ relative to $V_{SS}$	$V_{T1}$	-0.5 to 4.6	V
Voltage on any other pin relative to $V_{SS}$	$V_{T2}$	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	$T_A$	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	$T_{STG}$	-65 to 150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

#### TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High – Z	High – Z	$I_{SB1}$
	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	L	X	High – Z	High – Z	$I_{CC}, I_{CC1}$
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	$D_{OUT}$	High – Z	$I_{CC}, I_{CC1}$
	L	L	H	H	L	High – Z	$D_{OUT}$	
	L	L	H	L	L	$D_{OUT}$	$D_{OUT}$	
Write	L	X	L	L	H	$D_{IN}$	High – Z	$I_{CC}, I_{CC1}$
	L	X	L	H	L	High – Z	$D_{IN}$	
	L	X	L	L	L	$D_{IN}$	$D_{IN}$	

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.



#### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>*4</sup>	MAX.	UNIT		
Supply Voltage	V <sub>CC</sub>		2.7	3.0	3.6	V		
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>		2.2	-	V <sub>CC</sub> +0.3	V		
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>		-0.2	-	0.6	V		
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA		
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.2	2.7	-	V		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# ≤ 0.2V, I <sub>I/O</sub> = 0mA Others at 0.2V or V <sub>CC</sub> -0.2V	-45	-	12	20	mA	
			-55	-	10	17	mA	
	I <sub>CC1</sub>	Cycle time = 1μs CE# = 0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-	3	5	mA		
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	SL <sup>*5</sup>	25°C	-	1	3	μA
			SLI <sup>*5</sup>	40°C	-	1	3	μA
			SL		-	1	10	μA
			SLI		-	1	15	μA

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V

#### CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

#### AC TEST CONDITIONS

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA

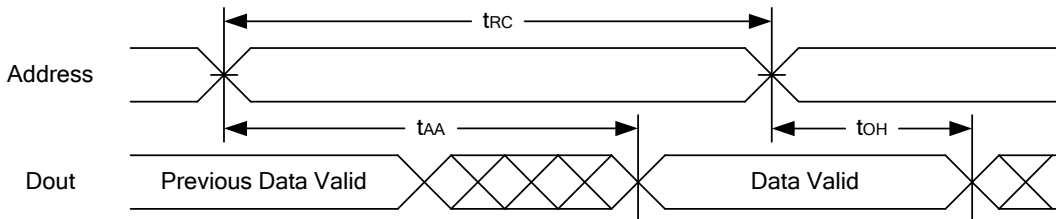
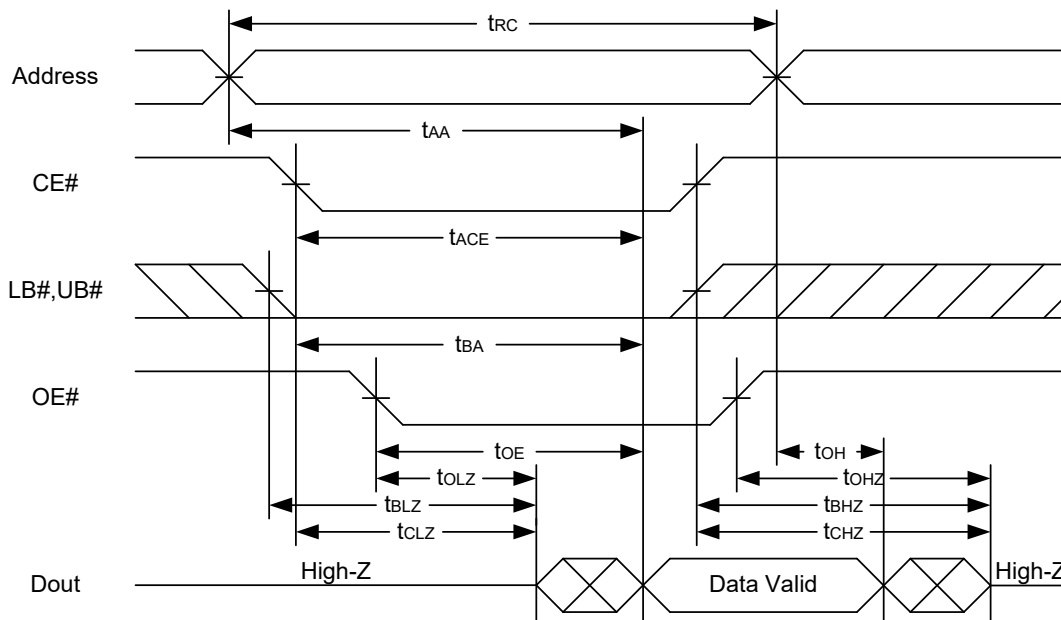
**AC ELECTRICAL CHARACTERISTICS**
**(1) READ CYCLE**

PARAMETER	SYM.	LY69L6416A-45		LY69L6416A-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	45	-	55	-	ns
Address Access Time	t <sub>AA</sub>	-	45	-	55	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	45	-	55	ns
Output Enable Access Time	t <sub>OE</sub>	-	25	-	30	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	10	-	10	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	5	-	5	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	15	-	20	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	15	-	20	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	ns
LB#, UB# Access Time	t <sub>BA</sub>	-	45	-	55	ns
LB#, UB# to High-Z Output	t <sub>BHZ</sub> *	-	20	-	25	ns
LB#, UB# to Low-Z Output	t <sub>BLZ</sub> *	10	-	10	-	ns

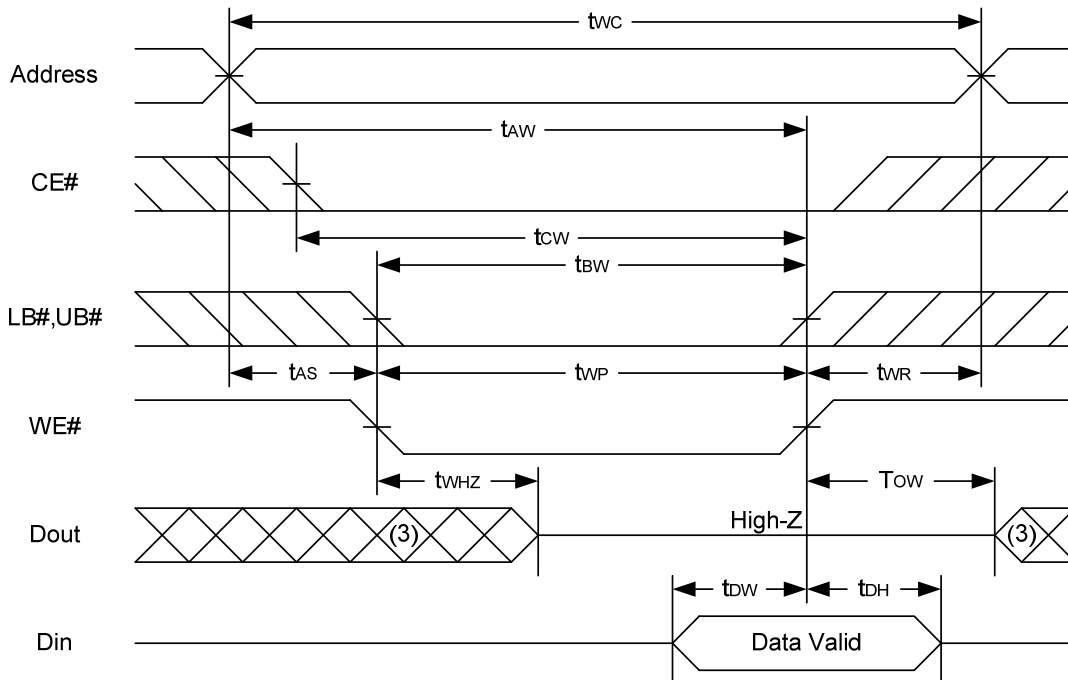
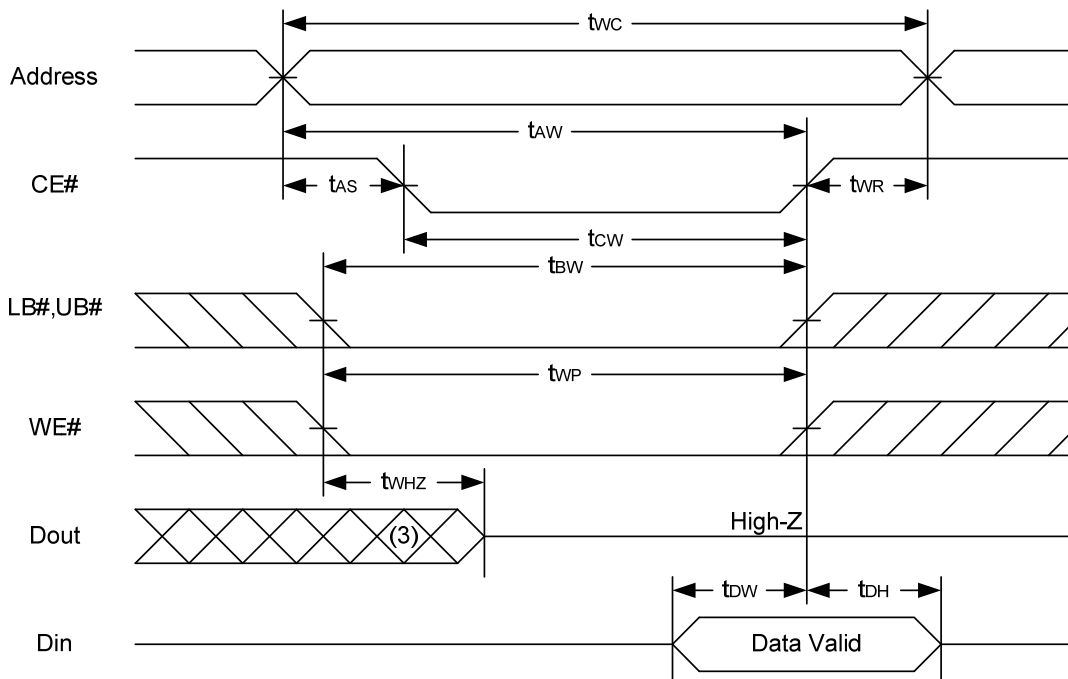
**(2) WRITE CYCLE**

PARAMETER	SYM.	LY69L6416A-45		LY69L6416A-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	45	-	55	-	ns
Address Valid to End of Write	t <sub>AW</sub>	40	-	50	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	40	-	50	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	35	-	45	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	20	-	25	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	5	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	15	-	20	ns
LB#, UB# Valid to End of Write	t <sub>BW</sub>	35	-	45	-	ns

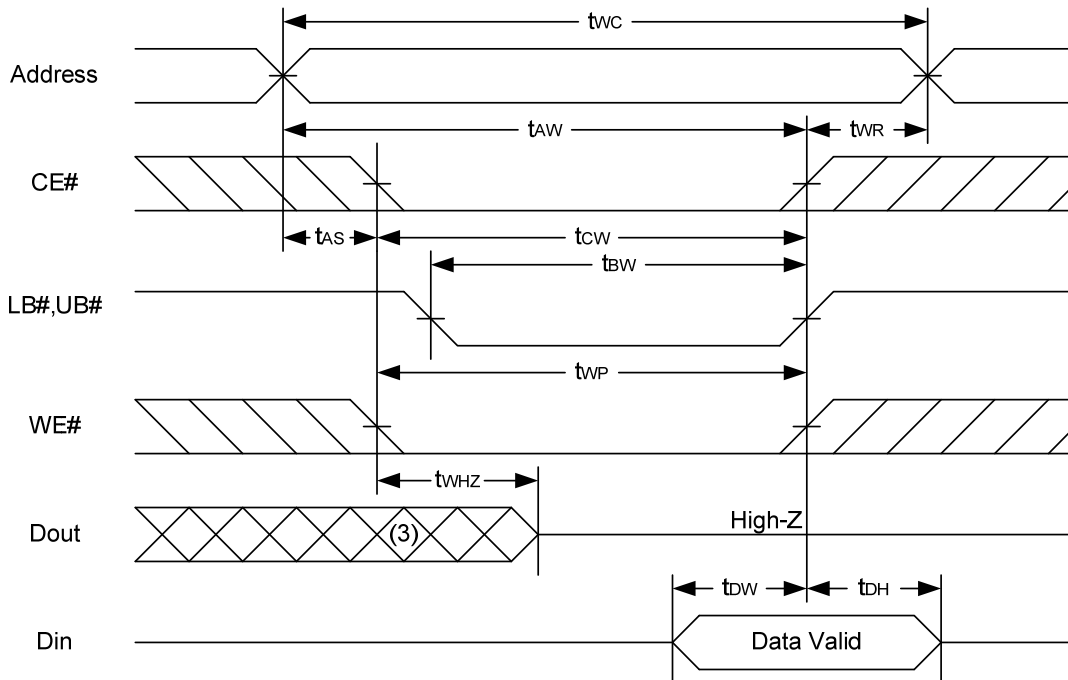
\*These parameters are guaranteed by device characterization, but not production tested.

**TIMING WAVEFORMS**
**READ CYCLE 1 (Address Controlled) (1,2)**

**READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)**

**Notes :**

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)**

**WRITE CYCLE 2 (CE# Controlled) (1,4,5)**




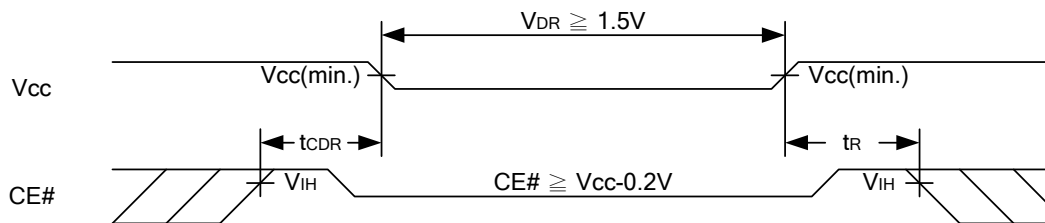
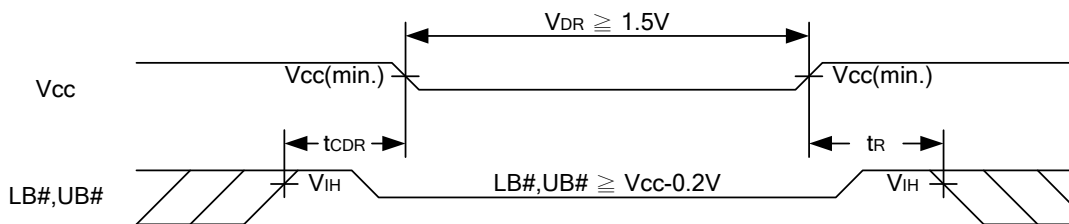
**WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)**

**Notes :**

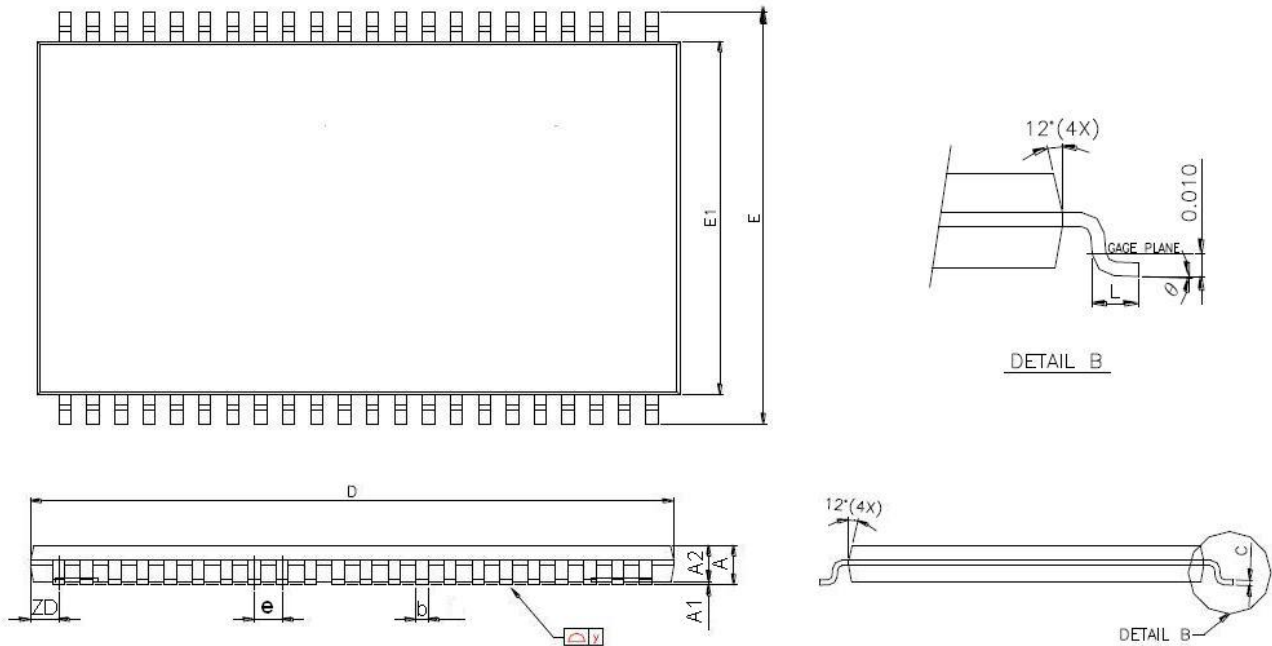
1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.

**DATA RETENTION CHARACTERISTICS**

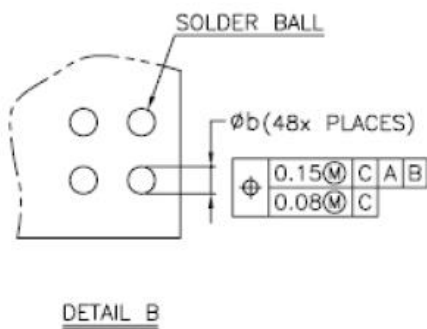
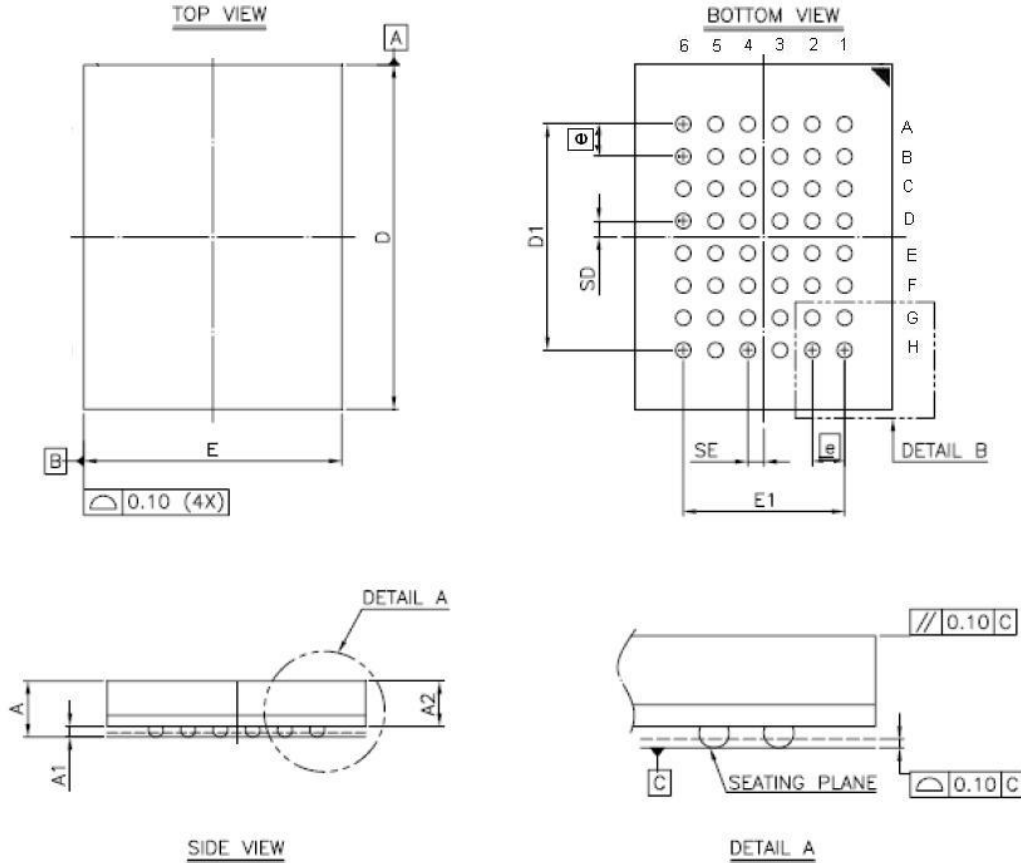
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	1.5	-	3.6	V		
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	SL	25°C	-	1	3	μA
			SLI	40°C	-	1	3	μA
		SL		-	1	5	μA	
		SLI		-	1	10	μA	
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns		

 t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**
**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**

**Low V<sub>CC</sub> Data Retention Waveform (2) (LB#, UB# controlled)**


**PACKAGE OUTLINE DIMENSION**
**44-pin 400mil TSOP II Package Outline Dimension**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

**48-ball 6mm × 8mm TFBGA Package Outline Dimension**


SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
⊠	0.75 BSC			0.030 BSC		

**NOTE:**

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44-pin(400 mil) TSOP II	45	Special Ultra Low Power	0°C~70°C	Tray	LY69L6416AML-45SL
				Tape Reel	LY69L6416AML-45SLT
			-40°C~85°C	Tray	LY69L6416AML-45SLI
				Tape Reel	LY69L6416AML-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY69L6416AML-55SL
				Tape Reel	LY69L6416AML-55SLT
			-40°C~85°C	Tray	LY69L6416AML-55SLI
				Tape Reel	LY69L6416AML-55SLIT
48-ball (6mm x 8mm) TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY69L6416AGL-45SL
				Tape Reel	LY69L6416AGL-45SLT
			-40°C~85°C	Tray	LY69L6416AGL-45SLI
				Tape Reel	LY69L6416AGL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY69L6416AGL-55SL
				Tape Reel	LY69L6416AGL-55SLT
			-40°C~85°C	Tray	LY69L6416AGL-55SLI
				Tape Reel	LY69L6416AGL-55SLIT



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